ADM6926/X

26 Port 10/100 Mbit/s Ethernet Switch Controller

ADM6926/X

Communications

Never stop thinking.

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ADM6926/X, 26 Port 10/100 Mbit/s Ethernet Switch Controller

Revision History: 2005-11-25, Rev. 1.03

Previous Version:

Page/Date	Subjects (major changes since last revision)
2003-08-08	Rev. 1.0, First release of ADM6926
2003-10-21	Rev. 1.01, Updated section 3.1.22
2003-12-01	Rev. 1.02, Updated sections 3.1.25, 4.2.10
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2005-11-25	Minor change. Included Green package information

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1 Product Overview

1.1 Overview

The ADM6926/X is a high performance/low cost, twenty six-port 10/100 Mbit/s Ethernet Switch Controller with all ports supporting 10/100 Mbit/s full duplex switch function. The ADM6926/X is intended for applications to standalone-bridge for the low cost ether-switch market. ADM6926/X can be programmed trunking port active. The trunking port can be connected to server or stacking two switch boxes to enhance the performance. The ADM6926X is the environmentally friendly “green” package version.

The ADM6926/X also supports back-pressure in half duplex mode and 802.3x flow control in full duplex mode. When back-pressure is enabled, and there is no receive buffer available for the incoming packet, the ADM6926/X will force a JAM pattern on the receiving port in half duplex mode and transmit the 802.3x packet back to receiving end in full duplex mode.

An intelligent address recognition algorithm makes ADM6926/X to recognize up to 4096 different MAC addresses and enables filtering and forwarding at full wire speed.

The ADM6926/X has embedded SRAM for the proprietary buffer management. The SRAM is used to store the incoming/outgoing packets. These buffers provide elastic storage for transferring data between low-speed and high-speed segments and buffers are efficiently allocated to improve the efficiency.

1.2 Features

- Supports twenty four 10/100M auto-detect Half/Full duplex switch ports with SS-SMII interface and two 10/100M Half/Full duplex port with RMII/MII interface
- Supports up to 4096 MAC addresses table (4-way hashing)
- Supports two queue for QOS (1:2 or 1:4 or 1:8 or 1:16)
- Supports Port-base, 802.1p and IP TOS priority
- Supports store & forward architecture and Performs forwarding and filtering at non-blocking full wire speed
- Supports buffer allocation with 256 bytes each
- Supports aging function and 802.3x flow control for full duplex and back-pressure function for half duplex operation in case buffer is full
- Supports packet length up to 1536 bytes
- Supports Congestion Flow Control
- Broadcast storm filter and Alert LED
- Port-base VLAN and adjustable VLAN to support up to 32 VLAN group
- Serial CPU interface for counter and port status output
- CPU can see-through to access PHY
- Flexible port trunking on fault tolerance and load balance
- Per port 32 bits smart counter for Rx/Tx byte/packet count, error count and collision count
- Rate-limit control (64K/128K/256K/512K/1M/4M/10M/20M)
- Per port auto learning enable/disable and if disable, forward non-learned packet to CPU
- MAC address table accessible (in each entry, reserve one bit for CPU to enable/disable aging out)
- Forward special multicast, BPDU, GMRP, GVRP and IGMP packets to CPU port
- 128-pin QFP package with 3.3 V/1.8 V power supply

1.3 Package Information

Product Name	Product Type	Package	Ordering Number
Ethernet Switch Controller	ADM6926/X	P-FQFP-128-1?	Q67801H 18A202[1)]

1) contact Infineon for the updated ordering information

1.4 Data Lengths

- qword: 64 bits
- dword: 32 bits
- word: 16 bits
- byte: 8 bits
- nibble: 4 bits

1.5 Block Diagram

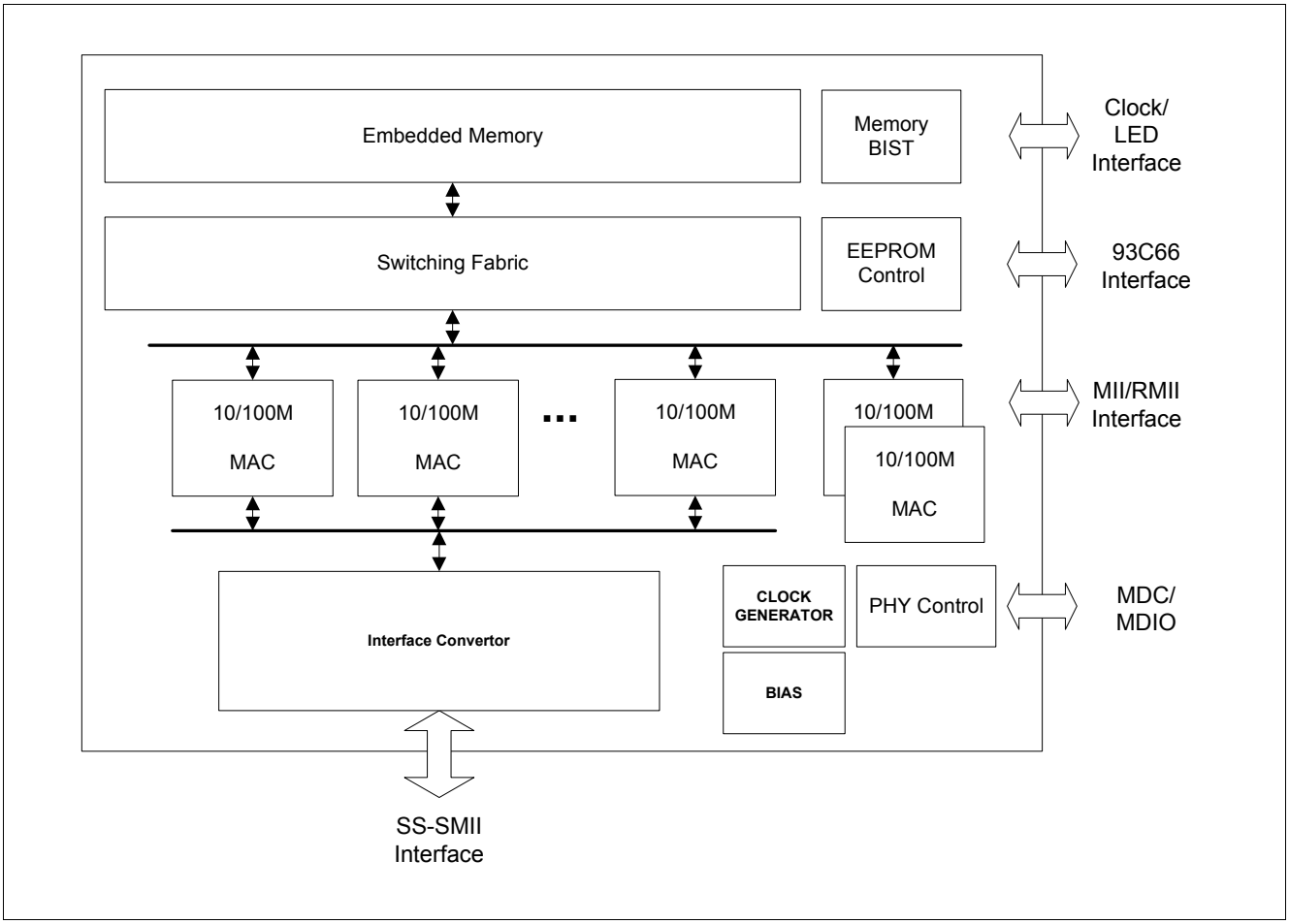


Figure 1 ADM6926/X Block Diagram

2 Interface Description

2.1 Pin Diagram

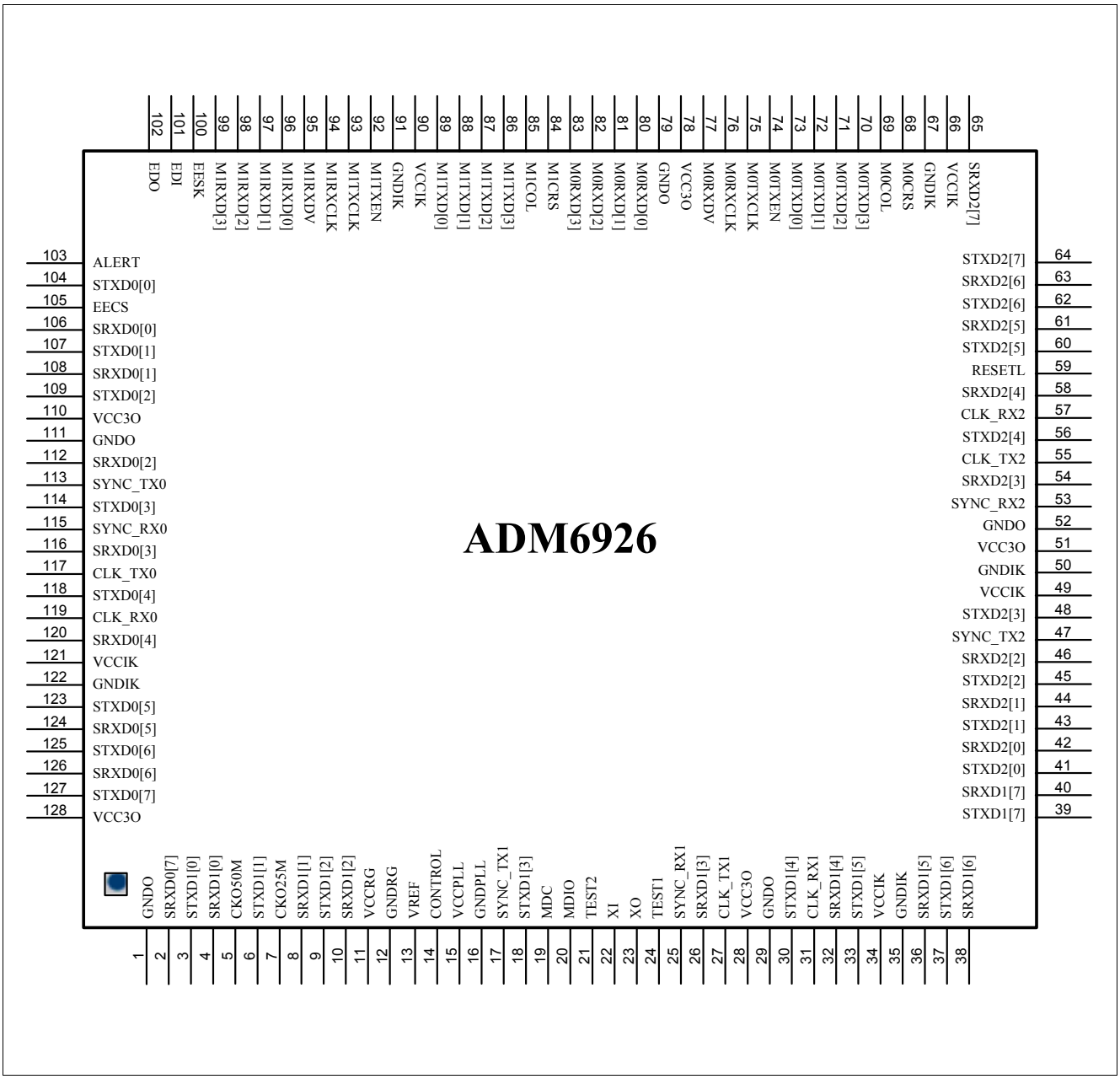


Figure 2 ADM6926/X Pin Diagram (SS-SMII Interface)

2.2 Abbreviations

Standard abbreviations for I/O tables:

Table 1 Abbreviations for Pin Type

Abbreviations	Description
I	Standard input-only pin. Digital levels.
O	Output. Digital levels.
I/O	I/O is a bidirectional input/output signal.
AI	Input. Analog levels.
AO	Output. Analog levels.
AI/O	Input or Output. Analog levels.
PWR	Power
GND	Ground
MCL	Must be connected to Low (JEDEC Standard)
MCH	Must be connected to High (JEDEC Standard)
NU	Not Usable (JEDEC Standard)
NC	Not Connected (JEDEC Standard)

Table 2 Abbreviations for Buffer Type

Abbreviations	Description
Z	High impedance
PU1	Pull up, 10 kΩ
PD1	Pull down, 10 kΩ
PD2	Pull down, 20 kΩ
TS	Tristate capability: The corresponding pin has 3 operational states: Low, high and high-impedance.
OD	Open Drain. The corresponding pin has 2 operational states, active low and tristate, and allows multiple devices to share as a wire-OR. An external pull-up is required to sustain the inactive state until another agent drives it, and must be provided by the central resource.
OC	Open Collector
PP	Push-Pull. The corresponding pin has 2 operational states: Active-low and active-high (identical to output with no type attribute).
OD/PP	Open-Drain or Push-Pull. The corresponding pin can be configured either as an output with the OD attribute or as an output with the PP attribute.
ST	Schmitt-Trigger characteristics
TTL	TTL characteristics

2.3 Pin Description

ADM6926/X pins are categorized into one of the following groups:

- SS-SMII Networking Interface, 60 pins
- MII/RMII Interface, 28 pins
- Power/Ground
- Miscellaneous pins, 16 pins

Table 3 I/O Signals

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
SS-SMII Networking Interface, 60 pins				
106	SRXD0_0	I	TTL	**Port 0 to Port 7 SS-SMII Receive Data Bit** The receive data should be synchronous to the rising edge of CLK_RX0.
108	SRXD0_1			
112	SRXD0_2			
116	SRXD0_3			
120	SRXD0_4			
124	SRXD0_5			
126	SRXD0_6			
2	SRXD0_7			
115	SYNC_RX0	I	TTL	**Port 0 to Port 7 SS-SMII Synchronous Signal** This signal is synchronous to the rising edge of CLK_RX0. Active high indicates the byte boundary.
119	CLK_RX0	I	TTL	**Reference Receive Clock for Port 0 to Port 7** This signal is 125 MHz input for SS-SMII interface.
104	STXD0_0	O	TTL, 8 mA	**Port 0 to Port 7 SS-SMII Transmit Data Bit** The transmit data is synchronous to the rising edge of CLK_TX0.
107	STXD0_1			
109	STXD0_2			
114	STXD0_3			
118	STXD0_4			
123	STXD0_5			
125	STXD0_6			
127	STXD0_7			
113	SYNC_TX0	O	TTL, 8 mA	**Port 0 to Port 7 SS-SMII Synchronous Signal** This signal is synchronous to the rising edge of CLK_TX0. Active high indicates the byte boundary.
117	CLK_TX0	O	TTL, 16 mA	**Reference Transmit Clock for Port 0 to Port 7** This signal is 125 MHz output for SS-SMII interface.
4	SRXD1_0	I	TTL	**Port 8 to Port 15 SS-SMII Receive Data Bit** The receive data should be synchronous to the rising edge of CLK_RX1.
8	SRXD1_1			
10	SRXD1_2			
26	SRXD1_3			
32	SRXD1_4			
36	SRXD1_5			
38	SRXD1_6			
40	SRXD1_7			
25	SYNC_RX1	I	TTL	**Port 8 to Port 15 SS-SMII Synchronous Signal** This signal is synchronous to the rising edge of CLK_RX1. Active high indicates the byte boundary.
31	CLK_RX1	I	TTL	**Reference Receive Clock for Port 8 to Port 15** This signal is 125 MHz input for SS-SMII interface.

Table 3 I/O Signals (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
3	STXD1_0	O	TTL, 8 mA	**Port 8 to Port 15 SS-SMII Transmit Data Bit** The transmit data is synchronous to the rising edge of CLK_TX1.
6	STXD1_1			
9	STXD1_2			
18	STXD1_3			
30	STXD1_4			
33	STXD1_5			
37	STXD1_6			
39	STXD1_7			
17	SYNC_TX1	O	TTL, 8 mA	**Port 8 to Port 15 SS-SMII Synchronous Signal** This signal is synchronous to the rising edge of CLK_TX1. Active high indicates the byte boundary.
27	CLK_TX1	O	TTL, 16 mA	**Reference Transmit Clock for Port 8 to Port 15** This signal is 125 MHz output for SS-SMII interface.
42	SRXD2_0	I	TTL	**Port 16 to Port 23 SS-SMII Receive Data Bit** The receive data should be synchronous to the rising edge of CLK_RX2.
44	SRXD2_1			
46	SRXD2_2			
54	SRXD2_3			
58	SRXD2_4			
61	SRXD2_5			
63	SRXD2_6			
65	SRXD2_7			
53	SYNC_RX2	I	TTL	**Port 16 to Port 23 SS-SMII Synchronous Signal** This signal is synchronous to the rising edge of CLK_RX2. Active high indicates the byte boundary.
57	CLK_RX2	I	TTL	**Reference Receive Clock for Port 16 to Port 23** This signal is 125 MHz input for SS-SMII interface.
41	STXD2_0	O	TTL, 8 mA	**Port 16 to Port 23 SS-SMII Transmit Data Bit** The transmit data is synchronous to the rising edge of CLK_TX2.
43	STXD2_1			
45	STXD2_2			
48	STXD2_3			
56	STXD2_4			
60	STXD2_5			
62	STXD2_6			
64	STXD2_7			
47	SYNC_TX2	O	TTL, 8 mA	**Port 16 to Port 23 SS-SMII Synchronous Signal** This signal is synchronous to the rising edge of CLK_TX2. Active high indicates the byte boundary.
55	CLK_TX2	O	TTL, 16 mA	**Reference Transmit Clock for Port 16 to Port 23** This signal is 125 MHz output for SS-SMII interface.
MII/RMII Interface, 28 pins				
68	M0CRS	I	TTL, PD	**MII Port0 Carrier Sense** This pin is internal pull-down.

Table 3 I/O Signals (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
69	M0COL	I	TTL, PD	**MII Port0 Collision Input** This pin is internal pull-down.
73	M0TXD_0	I/O	TTL, 8 mA, PD	**MII Port 0 Transmit Data Bit[0:3]** Synchronous to the rising edge of M0TXCLK. **RMII Port 0 Transmit Data Bit[0:1]** Synchronous to the rising edge of M0RXCLK. **RMIIMODE[1]**: Value on M0TXD_3 will be latched at the rising edge of RESETL to configure port 25 as RMII mode. **RMIIMODE[0]**: Value on M0TXD[2] will be latched at the rising edge of RESETL to configure port 24 as RMII mode.
72	M0TXD_1			
71	M0TXD_2			
70	M0TXD_3			
74	M0TXEN	I/O	TTL, 8 mA, PD	**MII/RMII Port 0 Transmit Enable** AGDIS. Value on this pin will be latched at the rising edge of RESETL to set aging disable.
75	M0TXCLK	I	TTL, PD	**MII Port 0 Transmit Clock Input** This pin is 25 MHz input for MII interface.
76	M0RXCLK	I	TTL, PD	**MII/RMII Port 0 Receive Clock Input** This pin is 25 MHz input for MII interface and 50 MHz REFCLK input for RMII interface.
77	M0RXDV	I	TTL, PD	**MII Port 0 Receive Data Valid** **RMII Port 0 Carrier Sense/Receive Data Valid** This pin is internal pull-down.
80	M0RXD_0	I	TTL, PD	**MII Port 0 Receive Data Bit[0:3]** **RMII Port 0 Receive Data Bit[0:1]** If in RMII mode, M0RXD_3 used for ext_dup_enable and M0RXD_2 used for ext_dup_full. Internal pull-down. See Sec3.1.27 for details.
81	M0RXD_1			
82	M0RXD_2			
83	M0RXD_3			
84	M1CRS	I	TTL, PD	**MII Port 1 Carrier Sense** This pin is internal pull-down.
85	M1COL	I	TTL, PD	**MII Port 1 Collision Input** This pin is internal pull-down.
89	M1TXD_0	I/O	TTL, 8 mA	**MII Port 1Transmit Data Bit[0:3]** Synchronous to the rising edge of M1TXCLK. **RMII Port 1Transmit Data Bit[0:1]** Synchronous to the rising edge of M1RXCLK. **BPEN**. Value on M1TXD[3] will be latched at the rising edge of RESETL to set Back_pressure enable. Internal pull-up. **FCEN**. Value on M1TXD[2] will be latched at the rising edge of RESETL to set flow control enable. Internal pull-up. **TNKEN**. Value on M1TXD[1] will be latched at the rising edge of RESETL to set trunking enable. Internal pull-up. **IPGLVING**. Value on M1TXD[0] will be latched at the rising edge of RESETL to set shorter IPG. Internal pull-down.
88	M1TXD_1			
87	M1TXD_2			
86	M1TXD_3			
92	M1TXEN	O	TTL, 8 mA, PU	**MII Port 1 Transmit Enable** ANEN. Value on this pin will be latched at the rising edge of RESETL to set auto_negotiation enable. Internal pull-up.

Table 3 I/O Signals (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
93	M1TXCLK	I	TTL, PD	**MII Port1 Transmit Clock Input** This signal is 25 MHz input for MII interface.
94	M1RXCLK	I	TTL, PD	**MII1 Receive Clock Input** This signal is 25 MHz input for MII interface and 50 MHz REFCLK input for RMII interface.
95	M1RXDV	I	TTL, PD	**MII/RMII Port 1 Receive Data Valid** This pin is internal pull-down.
96	M1RXD_0	I	TTL PD	**MII Port 1 Receive Data Bit[0:3]** **RMII Port 1 Receive Data Bit[0:1]** If in RMII mode, M1RXD_3 used for ext_dup_enable and M1RXD_2 used for ext_dup_full. Internal pull-down. See Sec3.1.27 for details.
97	M1RXD_1			
98	M1RXD_2			
99	M1RXD_3			
Power/Ground				
12	GNDRG	Analog GND	–	**Ground for Regulator**
11	VCCRG	Analog PWR	–	**3.3 V Power Supply for Regulator**
16	GNDPLL	Analog GND	–	**Ground for PLL**
15	VCCPLL	Analog PWR	–	**1.8 V Power Supply PLL**
35, 50, 67, 91, 122	GNDIK	Digital GND	–	**Ground for Core Logic**
34, 49, 66, 90, 121	VCCIK	Digital PWR	–	**1.8 V Power Supply for Core Logic**
1, 29, 52, 79, 111	GNDO	Digital GND	–	**Ground for I/O PAD**
28, 51, 78, 110, 128	VCC3O	Digital PWR	–	**3.3 V Power Supply for I/O PAD**
Miscellaneous Pins, 16 pins				
7	CK25MO	O	TTL, 16 mA	**25 MHz Clock Output** This pin will drive out 25 MHz.
5	CK50MO	O	TTL, 16 mA	**50 MHz Clock Output** This pin will drive out 50 MHz.
	COL_LED_10M	O	TTL, 16 mA	**COL_LED_10M** This pin shows collision LED for 10M domain (see EEPROM Register 1ch, Bit[9]).
22	XI	AI	–	**Crystal or OSC 50 MHz Input** This is the clock source of PLL. The PLL will generate 125 MHz for SS-SMII and 50 MHz for RMII and 25 MHz for MII.
23	XO	AO	–	**Crystal 50 MHz Output**

Table 3 I/O Signals (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
59	RESETL	I	TTL, ST	**Reset Signal** An active low signal with minimum 100 ms duration is required.
103	ALERT	O	TTL, 8 mA	**Alert LED Display** This pin will show the status of power-on-diagnostic and broadcast traffic.
	COL_LED_100M	O	TTL, 8 mA	**COL_LED_100M** This pin shows collision LED for 100M domain (see EEPROM Register 1ch, Bit[9]).
21	TEST_2	I	TTL, PD	**Industrial Test Pins** These pins are internal pull-down.
24	TEST_1			
19	MDC	O	TTL, 16 mA	**Management Data Clock** This pin output 2.2 MHz clock to drive PHY and access corresponding speed and duplex and link status through MDIO.
20	MDIO	I/O	TTL, 8 mA, PU	**Management Data** This pin is in-out to PHY. When RESETL is low, this pin will be tristate. This pin is internal pull-up.
100	EESK	I/O	TTL, 4 mA, PU	**EEPROM Serial Clock** This pin is clock source for EEPROM. When RESETL is low, it will be tristate. This pin is internal pull-up.
105	EECS	I/O	TTL, 4 mA, PD	**EEPROM Chip Select** This pin is chip enable for EEPROM. When RESETL is low, it will be tristate. This pin is internal pull-down.
101	EDI	I/O	TTL, 4 mA, PU	**EEPROM Serial Data Input** This pin is output for serial data transfer. When RESETL is low, it will be tristate. This pin is internal pull-up.
102	EDO	I	TTL, PU	**EEPROM Serial Data Output** This pin is input for serial data transfer. This pin is internal pull-up.
14	CONTROL	AO	–	**FET Control Signal** The pin is used to control FET for 3.3 V to 1.8 V regulator.
13	VREF	AI	–	**Regulator Control Input Signal**

3 Function Description

3.1 Introduction

The ADM6926/X uses a “store & forward” switching approach for the following reasons:

1. Store & forward switches allow switching between different speed media (e.g. 10BaseX and 100BaseX). Such switches require the large elastic buffers, especially bridging between a server on a 100Mbit/s network and clients on a 10 Mbit/s segment.
2. Store & forward switches improve overall network performance by acting as a “network cache”.
3. Store & forward switches prevent the forwarding of corrupted packets by the frame check sequence (FCS) before forwarding to the destination port.

3.1.1 Basic Operation

The ADM6926/X receives incoming packets from one of its ports, uses the source address (SA) and VID to update the address table, and then forwards the packet to the output ports determined by the destination address (DA) and VID.

If the DA and VID are not found in the address table, the ADM6926/X treats the packet as a broadcast packet and forwards the packet to the other ports within the same group.

The ADM6926/X automatically learns the port number of attached network devices by examining the SA and VID of all incoming packets. If the SA and VID are not found in the address table, the device adds it to the table.

3.1.2 Address Learning

The ADM6926/X provides two ways to create the entry in the address table: dynamic learning and manual learning. A four-way hash algorithm is implemented to allow 4 different addresses to be stored at the same location. Up to 4k entries can be created and all entries are stored in the internal SSRAM. Two parameters, SA and VID, are combined to generate the 10-bit hash key to allow that the same addresses with different port number can exist in the table at the same time.

Dynamic Learning

The ADM6926/X searches for SA and VID of an incoming packet in the address table and acts as follows:

If the SA+VID was not found in the address table (a new address), the ADM6926/X waits until the end of the packet (non-error packet) and updates the address table. If the SA+VID was found in the address table, then aging value of each corresponding entry will be reset to 0.

Dynamic learning will be disabled in the following condition:

1. Security violation happened.
2. The packet is a PAUSE frame.
3. The first bit of SA is 1_B.
4. The packet is an error packet (too long, too short or FCS error).
5. The CPU port leaning function is disabled or enabled but the CPU port instructs the switch not to learn the packet.
6. The port is in the Disabled or Blocking-not-Listening state in the Spanning Tree Protocol.

Manual Learning

The ADM6926/X implements the manual learning through the CUP’s help. The CPU can create or remove any entry in the address table. Each entry could be static or pointed to the output port map table. “Static” means the entry will not be aged forever. It is useful in the security function (forward unknown packets to the CPU port or discard) or monitor function (forward monitored address to the specific port). Output port map table is also helpful

in the IGMP function (if the number of the output port is more than one) or the users want to redirect the special packets with reserved DA.

3.1.3 Address Aging

The ADM6926/X will periodically (300 ms) remove the non-static address in the address table. This could help to prevent a station leaves the network and occupies a table space for a long time. Aging function can be disabled from the hardware pin.

3.1.4 Address Recognition and Packet Forwarding

The ADM6926/X forwards the incoming packets between bridge ports according to the DA and VID as follows:

Table 4 Address Recognition and Packet Forwarding

DA	DA+VID was found in the address table (entry not pointed to the output port map table)	DA+VID was found in the address table (entry pointed to the output port map table)	DA+VID was not found in the address table
Unicast Address	No Security Violation		
	Forward packets to the port determined by the address table. The packet may be dropped because of forwarding group boundary violation.	Forward packets to the ports determined by the output port map table constrained by the forwarding group.	Forward packets to the other ports within the same forwarding group.
	Security Violation		
	Drop or forward to CPU	Drop or forward to CPU	Drop or forward to CPU
Broadcast Address (All 1_B)	No Security Violation		
	Forwarding packets to the other ports within the same forwarding group.	Forward packets to the ports determined by the output port map table constrained by the forwarding group.	Forward packets to the other ports within the same forwarding group.
	Security Violation		
	Drop or forward to CPU	Drop or forward to CPU	Drop or forward to CPU
Reserved Address (01-80-c2-00-00-xx, with the option to forward normally)	No Security Violation		
	Forwarding packets to the other ports within the same forwarding group.	Forward packets to the ports determined by the output port map table constrained by the forwarding group.	Forward packets to the other ports within the same forwarding group.
	Security Violation		
	Same as the above	Same as the above	Same as the above
Reserved Address (01-80-c2-00-00-xx, with the option to forward to CPU)	No Security Violation		
	Forward the packet to the CPU port.	Forward the packet to the CPU port.	Forward the packet to the CPU port.
	Security Violation		
	Same as the above	Same as the above	Same as the above

Table 4 Address Recognition and Packet Forwarding (cont'd)

DA	DA+VID was found in the address table (entry not pointed to the output port map table)	DA+VID was found in the address table (entry pointed to the output port map table)	DA+VID was not found in the address table
Reserved Address (01-80-c2-00-00-xx, with the option to discard)	No Security Violation		
	Discard the packet.	Discard the packet.	Discard the packet.
	Security Violation		
	Same as the above	Same as the above	Same as the above
IGMP Packet (Port Enable IGMP)	No Security Violation		
	Forward the packet to the CPU port.	Forward the packet to the CPU port.	Forward the packet to the CPU port.
	Security Violation		
	Drop or forward to CPU	Drop or forward to CPU	Drop or forward to CPU
IGMP Packet (Port Disable IGMP)	No Security Violation		
	Forward packets to the port determined by the address table. The packet may be dropped because of forwarding group boundary violation.	Forward packets to the ports determined by the output port map table constrained by the forwarding group.	Forward packets according the Multicast Option.
	Security Violation		
	Drop or forward to CPU	Drop or forward to CPU	Drop or forward to CPU
Others	No Security Violation		
	Forward packets to the port determined by the address table. The packet may be dropped because of forwarding group boundary violation.	Forward packets to the ports determined by the output port map table constrained by the forwarding group.	Forward packets according the Multicast Option.
	Security Violation		
	Drop or forward to CPU	Drop or forward to CPU	Drop or forward to CPU

3.1.5 Trunking Port Forwarding

ADM6926/X supports the trunking forwarding and any port could be assigned to the trunking port. When one or more of the members link fail, the ADM6926/X will automatically change the transmit path from the failed link port to normal link port. Port based load balancing is implemented to distribute the loading.

3.1.6 Illegal Frames

The ADM6926/X will discard all illegal frames such as runt packet (less than 64 bytes), oversize packet (greater than 1518 or 1522 bytes) or bad CRC.

3.1.7 Back off Algorithm

The ADM6926/X implements the truncated exponential back off algorithm compliant to the 802.3 standard. ADM6926/X will restart the back off algorithm by choosing 0-9 collision count. After 16 consecutive retransmit trials, the ADM6926/X resets the collision counter.

3.1.8 Buffers and Queues

The ADM6926/X incorporates 26 transmit queues and receive buffer area for the 26 Ethernet ports. The receive buffers as well as the transmit queues are located within the ADM6926/X along with the switch fabric. The buffers are divided into 640 blocks of 256 bytes each. The queues of each port are managed according to each port's read/write pointer.

Input buffers and output queues are maintained through proprietary patent pending UNIQUE (Universal Queue management) scheme.

3.1.9 Half Duplex Flow Control

Back-pressure is supported for half-duplex operation.

When the ADM6926/X cannot allocate a receive buffer for an incoming packet (buffer full), the device will transmit a jam pattern on the port, thus forcing a collision.

3.1.10 Full Duplex Flow Control

When full duplex port runs out of its receive buffer, a PAUSE command will be issued by ADM6926/X to notice the packet sender to pause transmission. This frame based flow control is totally compliant to IEEE 802.3x. When flow control hardware pin is set to high during power on reset and per port PAUSE is enabled, ADM6926/X will output and accept 802.3x flow control packet.

3.1.11 Inter-Packet Gap (IPG)

IPG is the idle time between any two successive packets from the same port. The value is 9.6us for 10Mbit/s ETHERNET and 960ns for 100Mbit/s fast Ethernet.

3.1.12 Port VLAN or Tag VLAN Support

Two VLAN settings are supported by the ADM6926/X: the port-based VALN or the tag-based VLAN. For the port-based VLAN the ADM6926/X will use the port number as the index to lookup the forwarding table. For the tag-based VLAN, the ADM6926/X will use the VID to lookup the forwarding table. Each port is assigned a Port VID as the Default VID if tag-based VLAN is used. The ADM6926/X will check TAG, remove TAG, insert TAG, and re-calculate CRC if packet is changed.

Table 5 Packets Received are Untagged

Force no Tag	Bypass	Output Port is Tagged or not	Action
Don't Care	No	No	Untag as the original
	Yes	No	Untag as the original
	No	Yes	Add Tag
	Yes	Yes	Untag as the original

Table 6 Packets Received are Tagged

Force no Tag	Bypass	Output Port is Tagged or not	Action
No	No	No	The Tag is removed.
Yes	No	No	Tag as the original. The priority in the TAG header is not checked and VID will not change even if VID is 0 or 1.

Table 6 Packets Received are Tagged (cont'd)

Force no Tag	Bypass	Output Port is Tagged or not	Action
No	Yes	No	Tag as the original. The priority in the TAG header is checked and if the VID is 0 or 1, it may change to PVID (see EEPROM register 1ch, Bit[3]).
No	No	Yes	Tag as the original. The priority in the TAG header is checked and if the VID is 0 or 1, it may change to PVID (see EEPROM register 1ch, Bit[3]).
No	Yes	Yes	Tag as the original. The priority in the TAG header is checked and if the VID is 0 or 1, it may change to PVID (see EEPROM register 1ch, Bit[3]).
Yes	Yes	No	Tag as the original. The priority in the TAG header is not checked. The VID will not change.
Yes	No	Yes	The Tag will be added and packet will be double tagged output. The VID will not change.
Yes	Yes	Yes	Tag as the original. The priority in the TAG header is not checked. The VID will not change.

3.1.13 Priority Control

The ADM6926/X provides two priority queues on each output port. Five ways could be used to assign a priority to a packet.

1. The priority assigned to each receiving port
2. The priority field in the 802.1Q Tag Header
3. The IPv4 TOS field in the IPv4 Header
4. Priority assigned by the CPU
5. Management packet (high priority assigned)

3.1.14 Alert LED Display

Two functions are displayed through the Alert LED.

1. Diagnostic Mode after Power on
   a) After reset or power up, LED keeps on at least 3 second, and processes internal SSRAM self-test.
   b) If test passes, the ADM6926/X turns off LED and goes to the broadcast storm mode.
   c) If SSRAM test fails, the ADM6926/X turns off LED, then keeps on.
2. Broadcast Storm Mode after SSRAM Self-test. Packets with DA = 48'hffffffffffff will be counted into the storm counter.
   Two thresholds (rising and falling) are used to control the broadcast storm.
   a) Time Scale: 50ms is used. The max packet number in 100BaseT is 7490. The max packet number in 10BaseT is 749.
   b) Port Rising Threshold, see **Table 7**.
   c) Port Falling Threshold, see **Table 8**.

Table 7 Port Rising Threshold

Broadcast Storm Threshold	00	01	10	11
All 100TX	Disable	10%	20%	40%
Not All 100TX	Disable	1%	2%	4%

Table 8 Port Falling Threshold

Broadcast Storm Threshold	00	01	10	11
All 100TX	Disable	5%	10%	20%
Not All 100TX	Disable	0.5%	1%	2%

3.1.15 Broadcast Storm Filter

If broadcast storming filter is enabled, the broadcast packets (DA = 48'hffff-ffff-ffff) over the rising threshold within 50 ms will be discarded when the alert LED is turned on.

3.1.16 Collision LED Display

Two collision LEDs are supported. (see EEPROM Register 1ch, Bit[9])

1. 100M Collision LED. If collision happens in one of the ports configured 100M, the 100M Collision LED will flash in rate of 2 Hz.
2. 10M Collision LED. If collision happens in one of the ports configured 10M, the 10M Collision LED will flash in rate of 2 Hz.

3.1.17 Bandwidth Control

The ADM6926/X allows the user to limit the bandwidth for each input or output port. 64k, 128K, 256k, 512K, 1M, 4M, 10M and 20M are supported.

3.1.18 Smart Discard

The ADM6926/X supports a smart mechanism to discard packets early according to their priority to prevent the resource blocked by the low priority. The discard ratio is as follows:

Table 9 Discard Ratio

Discard Mode Utilization	00	01	10	11
00	0%	0%	0%	0%
01	0%	0%	25%	50%
11	0%	25%	50%	75%

3.1.19 Security Support

4 level security schemes are supported by the ADM6926/X. All the security violation address will not be automatically learned.

The violated packet could be forwarded to the CPU port for management or discarded. When CPU is not present, ADM6926/X also provides a simple way to lock the first address to prevent illegal address access.

3.1.20 Smart Counter Support

Six counters per port are supported by the ADM6926/X.

1. Receive Packet Count
2. Receive Packet Length Count
3. Transmit Packet Count
4. Transmit Packet Length Count
5. The Error Count
6. The Collision Count

3.1.21 Length 1536 Mode

The ADM6926/X provides a function to enable the port to receive packets up to 1536 Byte.

3.1.22 PHY Management (MDC/MDIO Interface)

The ADM6926/X uses the MDC/MDIO interface to set the PHY status. After the reset or power up, the MDC/MDIO controller will delay about 130 ms to wait for the PHY to ready. The ADM6926/X supports two ways to configure the PHY setting.

1. PHY master. The switch only reads the PHY status (speed, duplex, link, and pause). This mode is useful when users want to configure PHY through the CPU help. The ADM6926/X supports an indirect way (a PHY Control Register) for CPU to access PHYs.
2. PHY slave. The switch uses the EEPROM setting to control the PHY attached (only speed, duplex, link, and pause are supported). After the port setting changed, the ADM6926/X will use the new setting to program the PHY again and update the status. 8 commands are provided in this mode to allow the customer to customize the PHY setting.

Note: The PHY address attached to port 0 is 5'h8, the PHY address attached to port 1 is 5'h9, …, the PHY address attached to port 23 is 5'h1f, the PHY address attached to port 24 is 5'h6 and the PHY address attached to port 25 is 5'h7.

3.1.23 Forward Special Packets to the CPU Port (IGMP and Spanning Tree Support)

ADM6926/X will forward the special packets to the CPU port to provide the management function.

1. DA is 01-80-C2-00-00-00 (BPDU)
2. DA is 01-80-C2-00-00-02 (Slow Protocol)
3. DA is 01-80-C2-00-00-03 (802.1x PAE)
4. DA is 01-80-C2-00-00-04 ~ 01-80-C2-00-00-0f
5. DA is 01-80-C2-00-00-20 (GMRP)
6. DA is 01-80-C2-00-00-21 (GVRP)
7. DA is 01-80-C2-00-00-22 (GVRP)
8. DA is 01-00-5E-xx-xx-xx and protocol field is 2 for IPV4 (IGMP)

3.1.24 Special TAG

The ADM6926/X has an ability to insert 4Byte special TAG when packets transmitted to the CPU port or to remove 8Byte additional TAG in the packets when packets are received from the CPU port. The configuration is shown in the CPU Configuration Register. This special function allows the CPU to know the source port which will be used in the IGMP Snooping, Spanning Tree or the Security function. The CPU also could insert additional 8-byte Tag to instruct the switch to handle the packets. The packets format is as follows:

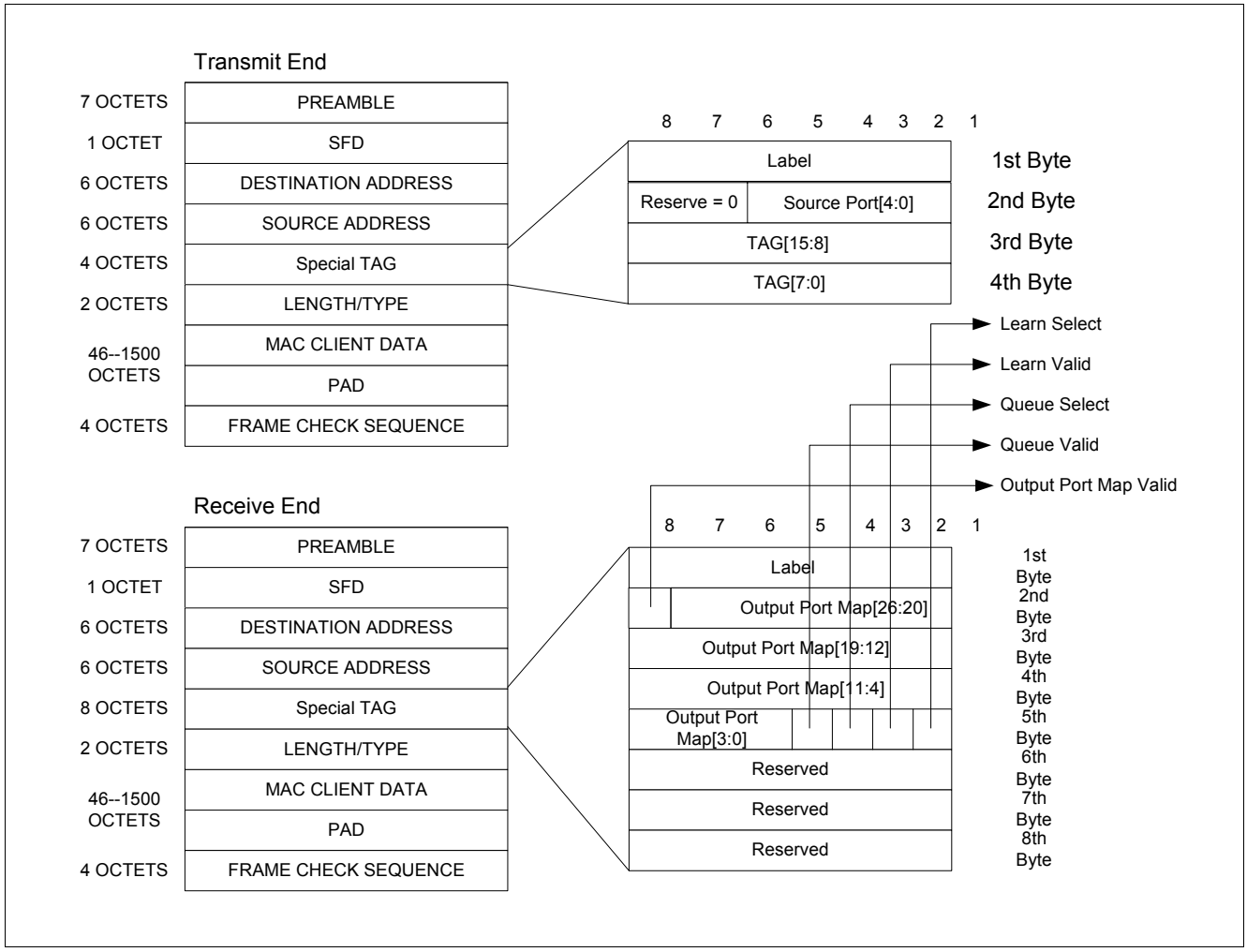


Figure 3 Packet Format

Table 10 Special TAG Fields

Configuration	Description	Default
Label	The field is used for CPU to decide if the special TAG is valid. If the switch finds the Label doesn't equal to the value assigned by the EEPROM, it must receive as the normal mode. This case exists when user wants the switch to insert 4 byte special tag even for Pause packets.	8'b0
Output Port Map Valid	1_B , The switch is instructed to override the switch operation. It will forward the packets following the Output Port Map field. 0_B , The switch will treat the packet as the normal mode.	1'b0

Table 10 Special TAG Fields (cont'd)

Configuration	Description	Default
Output Port Map[26:0]	Bit[26] = 1, the CPU wants to forward packets to more than 2 ports. Bit[26] = 0, the CPU wants to forward packets to only one port. Bit[x], x = 0 ~ 25, the CPU wants to forward packets to Port x. Example: 1. The CPU wants to forward packet to P1 and P2 then the Output Port Map is as follows: Bit 26, 25~24, 23~16, 15~8, 7~0 Map 1, 00, 0000_0000, 0000_0000, 0000_0110 2. The CPU wants to forward packets to P5 only. Bit 26, 25~24, 23~16, 15~8, 7~0 Map 0, 00, 0000_0000, 0000_0000, 0010_0000	27'h0
TAG[25:0]	This value is the same as the TAG header if the CPU port is configured to a TAG port.	16'h0
Source Port[4:0]	This field indicates the source port the packet comes from.	5'h0
Queue Valid	1_B , The switch is instructed to override the switch operation. It will forward the packets using the Queue Select Field. 0_B , The switch will treat the packets as the normal mode.	1'b0
Queue Select	1_B , Mapped for High Queue 0_B , Mapped for Low Queue	1'b0
Learn Valid	1_B , The switch is instructed to override the switch operation. The CPU port will use the Learn Field to decide how to learn the packet. 0_B , The switch will treat the packets as the normal mode. That is, the CPU port will learn or disable learning according the Disable CPU Port Learning Function configured in the CPU Control Register.	1'b0
Learn Select	1_B , Learn the packet 0_B , Don't learn the packet	1'b0

3.1.25 Port 24 and Port 25 Interface (Only SS-SMII Package Support)

Three interfaces in port 24 and port 25 are supported by the ADM6926/X: (1) MII Interface (2) RMII Interface.

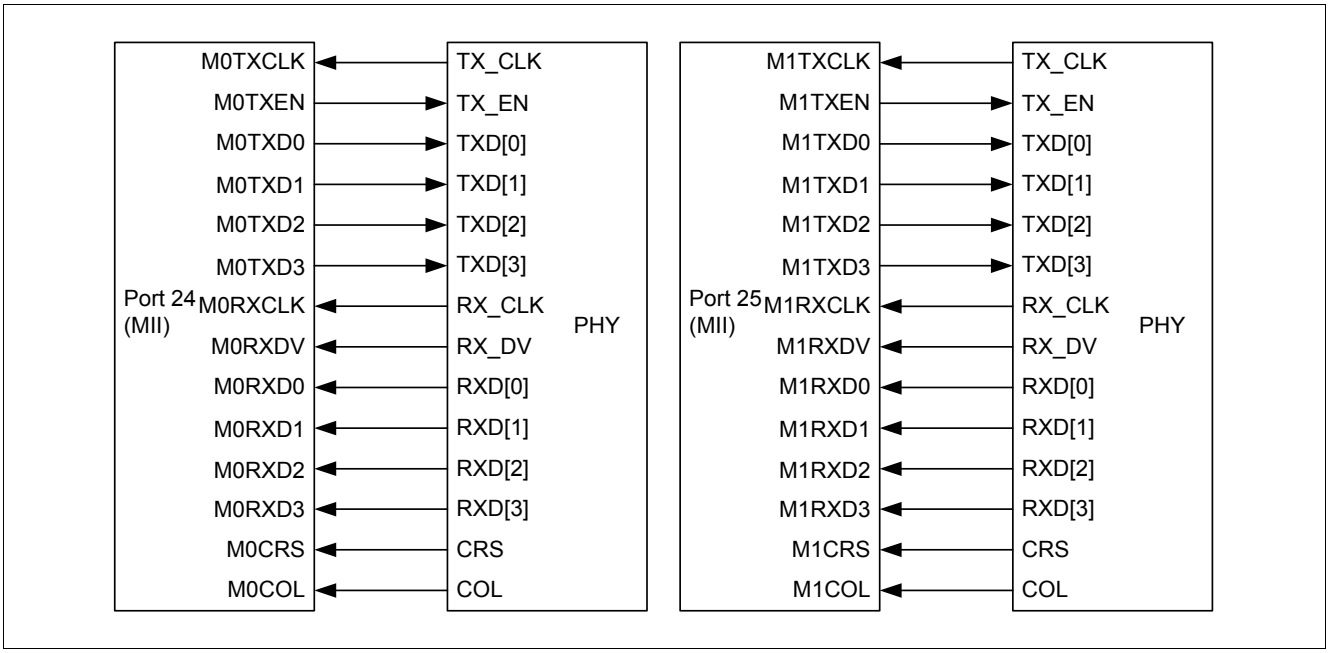


Figure 4 MII Interface Diagram

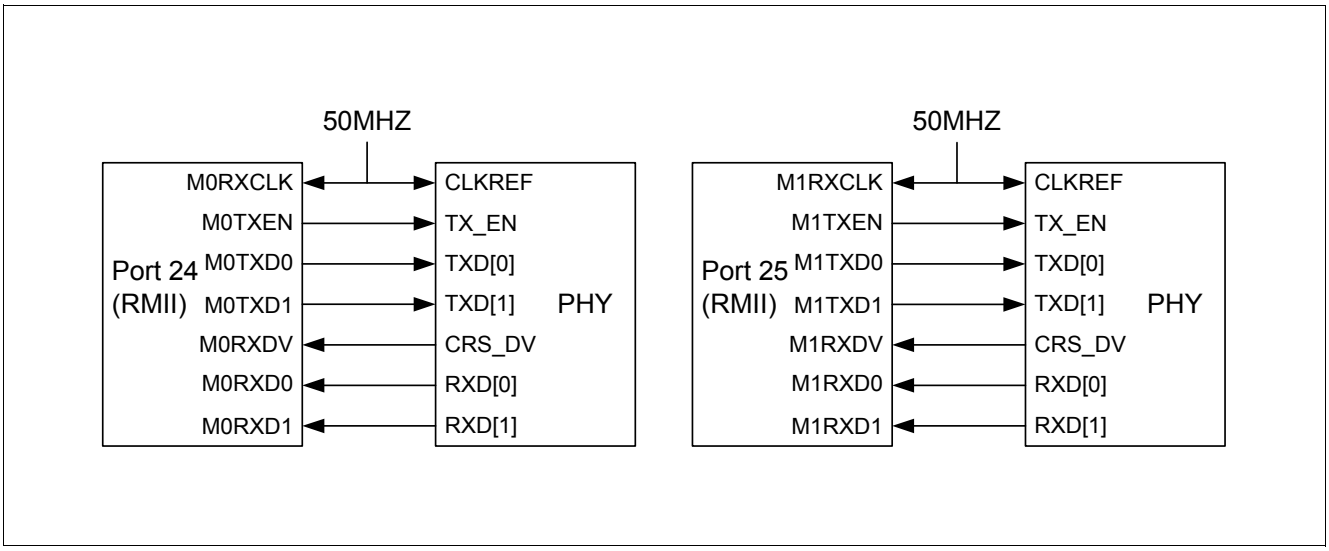


Figure 5 RMII Interface

3.1.26 Hardware, EEPROM and SMI Interface for Configuration

Three ways are supported to configure the setting in the ADM6926: (1) Hardware Setting (2) EERPROM InterfADM6926/Xace (3) SMI Interface. Users could use EEPROM and SMI interfaces combined with the CPU port to provide proprietary functions. Four pins are needed when using these two interfaces. See the following figure as a description.

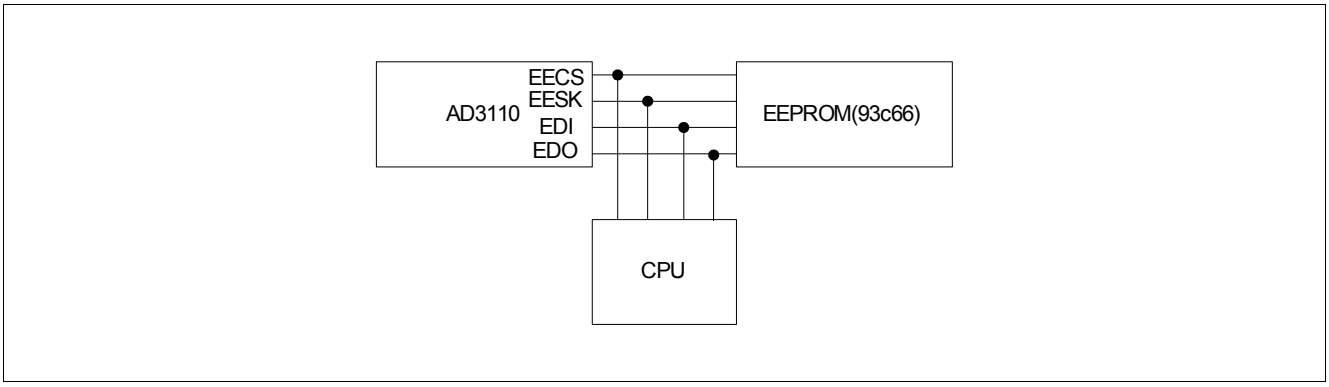


Figure 6 Hardware, EEPROM and SMI Interface Configuration

3.1.26.1 Hardware Setting

The ADM6926/X provides some hardware pins where values reside on during power on or reset will be strapped for the default setting.

Table 11 SS-SMII and RMII Pins

SS-SMII Pin Name	RMII Pin Name	Description
M1TXD0	M1TXD0	IPG Average 92 bit time. Internally Pulled Down. 0_B , Disable IPG Average 92 1_B , Enable IPG Average 92
M1TXD1	M1TXD1	Trunk En. Internally Pulled Up. 0_B , Trunking Disable. The ADM6926/X has no trunking function even if EEPROM sets. 1_B , Trunking Enable. Use EEPROM to configure the trunk member.
M1TXD2	M1TXD2	Pause. Internally Pulled Up. 0_B , The switch doesn't allow the Pause function even if EEPROM set. The only way to start the Pause function is through the CPU help. 1_B , The switch allows the Pause function. This function can be disabled by the EEPROM.
M1TXD3	M1TXD3	Back-Pressure. Internally Pulled Up. 0_B , The switch doesn't allow the Back-Pressure function even if EEPROM set. 1_B , The switch allows the Back-Pressure function. This function can be disabled by the EEPROM.
M1TXEN	M1TXEN	Auto-Neg En. Internally Pulled Up. 0_B , The switch doesn't allow Auto-Negotiation function even if EEPROM set. The only way to start the Auto-Negotiation function is through the CPU help. 1_B , The switch allows the Auto-Negotiation function. This function can be disabled by the EEPROM.
M0TXEN	M0TXEN	Aging Dis. Internally Pulled Down. 0_B , The switch will age the entry in the address table. 1_B , The switch will not age the entry in the address table.

Table 11 SS-SMII and RMII Pins (cont'd)

SS-SMII Pin Name	RMII Pin Name	Description
M0TXD0	Don't Support	Port 24 Interface Configuration
M0TXD2	Don't Support	M0TXD0, M0TXD2, Interface 0_B , 0, Port 24 is configured to MII in SS-SMII package (internal value). x_B , 1, Port 24 is configured to RMII in SS-SMII package.
M0TXD1	Don't Support	Port 25 Interface Configuration
M0TXD3	Don't Support	M0TXD1, M0TXD3, Interface configured to MII in SS-SMII package (internal value). x_B , 1, Port 25 is configured to RMII is SS-SMII package

When port 24 or port 25 is configured to RMII mode in SS-SMII package, we can use the hardware pins to configure duplex status of these two ports.

Table 12 Port 24 Duplex Configuration

M0RXD3	M0RXD2	Description
0	0	Duplex status is determined as port 0 ~ port 23.
0	1	Duplex status is determined as port 0 ~ port 23.
1	0	Full Duplex is determined.
1	1	Half Duplex is determined.

Table 13 Port 25 Duplex Configuration

M1RXD3	M1RXD2	Description
0	0	Duplex status is determined as port 0 ~ port 23.
0	1	Duplex status is determined as port 0 ~ port 23.
1	0	Full Duplex is determined.
1	1	Half Duplex is determined.

3.1.26.2 EEPROM Interface

The EEPROM Interface is provided so the users could easily configure the setting without CUP's help. Because the EEPROM Interface is the same as the 93c66, it also allows the CPU to write the EEPROM register and renew the 93c66 at the same time. After the power up or reset (default value from the hardware pins fetched in this stage), the ADM6926/X will automatically detect the presence of the EEPROM by reading the address 0 in the 96c66. If the value = 16'h4154, it will read all the data in the 93c66. If not, the ADM6926/X will stop loading the 93c66. The user also could pull down the EDO to force the ADM6926/X not to load the 93c66. The 93c66 loading time is around 30 ms. Then CPU should give the high-z value in the EECS, EESK and EDI pins in this period if we really want to use CPU to read or write the registers in the ADM6926/X.

The EEPROM Interface needs only one Write command to complete a writing operation. If updating the 93c66 at the same time is necessary, three commands Write Enable, Write, and Write Disable are needed to complete this job (See 93c66 Spec. for a reference). Users should note that the EERPOM interface only allows the CPU to write the EEPROM register in the ADM6926/X and doesn't support the READ command. If CPU gives the Read Command, ADM6926/X will not respond and 93c66 will respond with the value. Users should also note that one additional EESK cycle is needed between any continuous commands (Read or Write).

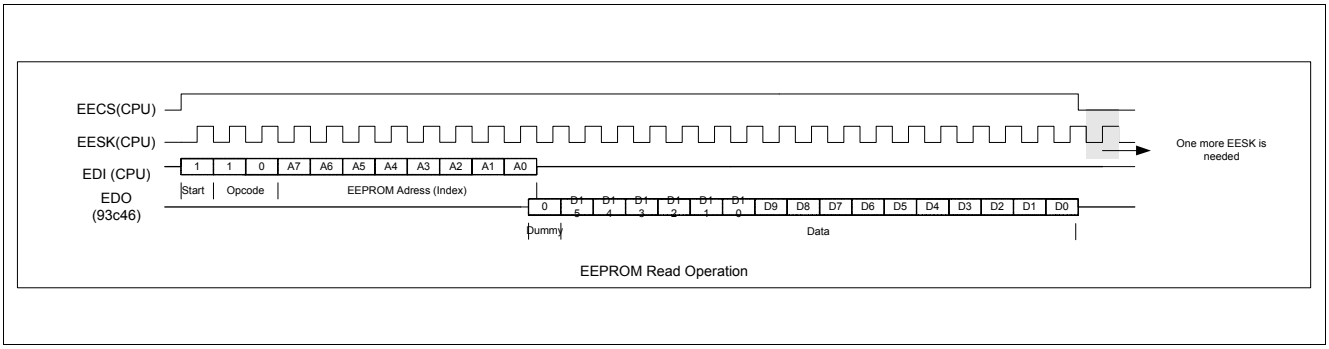


Figure 7 Read 93c66 via the EEPROM Interface (Index = 2, Data = 16'h1111)

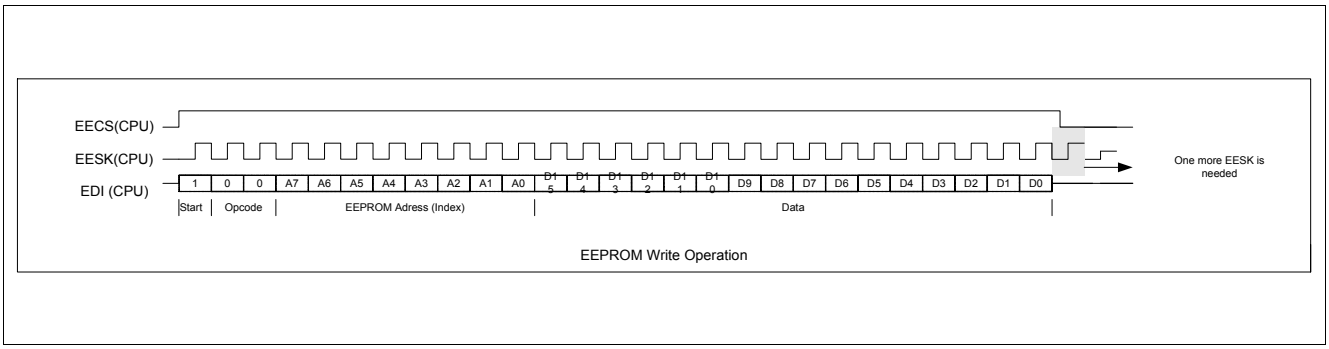


Figure 8 Write EEPROM Registers in the ADM6926/X (Index = 2, Data = 16'h2222)

3.1.26.3 SMI Interface

The SMI consists of two pins, management data clock (EESK) and management data input/output (EDI). The ADM6926/X is designed to support an EESK frequency up to 25 MHz. The EDI pin is bi-directional and may be shared with other devices. EECS pin may be needed (pulled to low) if EEPROM interface is also used.

The EDI pin requires a 1.5 k Ω pull-up which, during idle and turnaround periods, will pull EDI to a logic one state. ADM6926/X requires a single initialization sequence of 32 bits of preamble following power-up/hardware reset. The first 32 bits are preamble consisting of 32 contiguous logic one bits on EDI and 32 corresponding cycles on EESK. Following preamble is the start-of-frame field indicated by a <01> pattern. The next field signals the operation code (OP): <10> indicates read from management register operation, and <01> indicates write to management register operation. The next field is management register address. It is 10 bits wide and the most significant bit is transferred first.

During Read operation, a 2-bit turn around (TA) time spacing between the register address field and data field is provided for the EDI to avoid contention. Following the turnaround time, a 32-bit data stream is read from or written into the management registers of the ADM6926/X.

(A) Preamble Suppression

The SMI of ADM6926/X supports a preamble suppression mode. The ADM6926/X requires a single initialization sequence of 32 bits of preamble following power-up/hardware reset. This requirement is generally met by pulling-up the resistor of EDI While the ADM6926/X will respond to management accesses without preamble, a minimum of one idle bit between management transactions is required.

When ADM6926/X detects that there is address match, then it will enable Read/Write capability for external access. When address is mismatched, then ADM6926/X will tristate the EDI pin.

(B) Read Switch Register via SMI Interface (Offset Hex = 10'h2, Data = 32'h2600_0000)

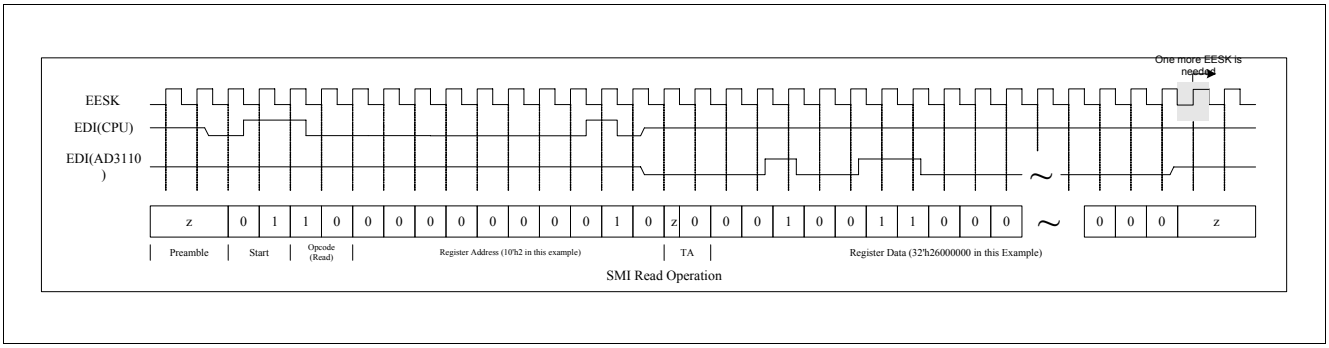


Figure 9 Read Switch Register via SMI Interface

(C) Write Switch Register via SMI Interface (Offset Hex = 10'h180, Data = 32'h1300_0000)

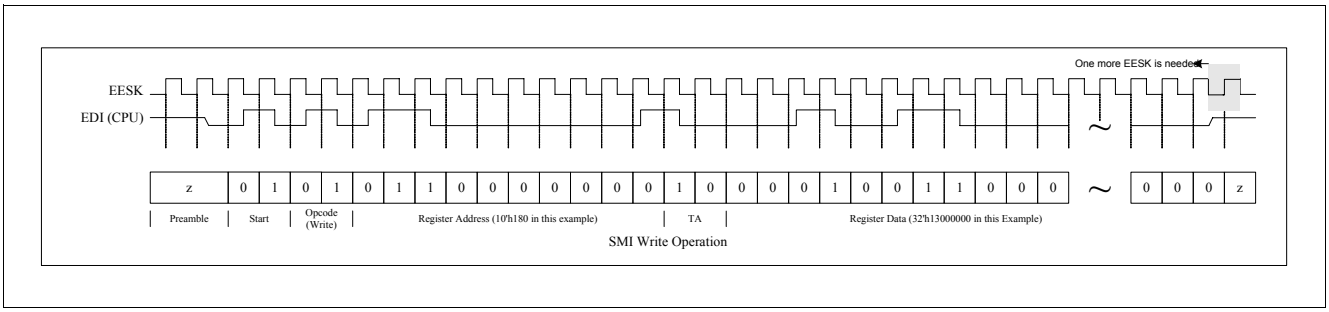


Figure 10 Write Switch Register via SMI Interface

(D) The Pin Type of EECS, EESK, EDI and EDO during the Operation

Table 14 Pin Type of EECS, EESK, EDI and EDO during Operation

Pin Name	Reset Operation	Load EEPROM	Write Operation	Read Operation
EECS	Input	Output	Input	Input
EESK	Input	Output	Input	Input
EDI	Input	Output	Input	Input / Output
EDO	Input	Input	Input	Input

3.2 EEPROM Register Format

The EEPROM can be auto-detected by ADM6926/X through the signature register. The ADM6926/X supports C66 EEPROM. After the EEPROM is loaded, the output pins of ADM6926/X are tristate and released to CPU. The release time is about 30ms after end of RESET. Whenever CPU modifies the setting of C66, the new value will be written to ADM6926/X at the same time. If CPU changes the port setting (Duplex/Speed/AEN), the ADM6926/X will restart the auto-negotiation automatically.

Table 15 EEPROM Format

Offset Hex		Index	Bit 15 - 8	Bit 7 - 0	Type	Default
0200_H	Low	0_H	Signature		ro	4154_H
0201_H	High	1_H	Global Configuration		rw	3800_H
0202_H	Low	2_H	Port 0 Configuration		rw	$80FF_H$
0203_H	High	3_H	Port 1 Configuration		rw	$80FF_H$

Table 15 EEPROM Format (cont'd)

Offset Hex		Index	Bit 15 - 8	Bit 7 - 0	Type	Default
0204_H	Low	4_H	Port 2 Configuration		rw	$80FF_H$
0205_H	High	5_H	Port 3 Configuration		rw	$80FF_H$
0206_H	Low	6_H	Port 4 Configuration		rw	$80FF_H$
0207_H	High	7_H	Port 5 Configuration		rw	$80FF_H$
0208_H	Low	8_H	Port 6 Configuration		rw	$80FF_H$
0209_H	High	9_H	Port 7 Configuration		rw	$80FF_H$
$020A_H$	Low	A_H	Port 8 Configuration		rw	$80FF_H$
$020B_H$	High	B_H	Port 9 Configuration		rw	$80FF_H$
$020C_H$	Low	C_H	Port10 Configuration		rw	$80FF_H$
$020D_H$	High	D_H	Port 11 Configuration		rw	$80FF_H$
020E	Low	E_H	Port 12 Configuration		rw	$80FF_H$
020f	High	F_H	Port 13 Configuration		rw	$80FF_H$
0210_H	Low	10_H	Port 14 Configuration		rw	$80FF_H$
0211_H	High	11_H	Port 15 Configuration		rw	$80FF_H$
0212_H	Low	12_H	Port 16 Configuration		rw	$80FF_H$
0213_H	High	13_H	Port 17 Configuration		rw	$80FF_H$
0214_H	Low	14_H	Port 18 Configuration		rw	$80FF_H$
0215_H	High	15_H	Port 19 Configuration		rw	$80FF_H$
0216_H	Low	16_H	Port 20 Configuration		rw	$80FF_H$
0217_H	High	17_H	Port 21 Configuration		rw	$80FF_H$
0218_H	Low	18_H	Port 22 Configuration		rw	$80FF_H$
0219_H	High	19_H	Port 23 Configuration		rw	$80FF_H$
$021A_H$	Low	$1A_H$	Port 24 Configuration		rw	$80FF_H$
$021B_H$	High	$1B_H$	Port 25 Configuration		rw	$80FF_H$
$021C_H$	Low	$1C_H$	Miscellaneous Configuration		rw	820_H
$021D_H$	High	$1D_H$	TOS Priority Map	VLAN Priority Map	rw	0_H
$021E_H$	Low	$1E_H$	Forwarding Group 0 Outbound Port Map Low		rw	$FFFF_H$
$021F_H$	High	$1F_H$	Forwarding Group 0 Outbound Port Map High		rw	$3FF_H$
0220_H	Low	20_H	Forwarding Group 1 Outbound Port Map Low		rw	$FFFF_H$
0221_H	High	21_H	Forwarding Group 1 Outbound Port Map High		rw	3FF
0222_H	Low	22_H	Forwarding Group 2 Outbound Port Map Low		rw	$FFFF_H$
0223_H	High	23_H	Forwarding Group 2 Outbound Port Map High		rw	$3FF_H$
0224_H	Low	24_H	Forwarding Group 3 Outbound Port Map Low		rw	$FFFF_H$
0225_H	High	25_H	Forwarding Group 3 Outbound Port Map High		rw	$3FF_H$
0226_H	Low	26_H	Forwarding Group 4 Outbound Port Map Low		rw	$FFFF_H$
0227_H	High	27_H	Forwarding Group 4 Outbound Port Map High		rw	$3FF_H$
0228_H	Low	28_H	Forwarding Group 5 Outbound Port Map Low		rw	$FFFF_H$
0229_H	High	29_H	Forwarding Group 5 Outbound Port Map High		rw	$3FF_H$
$022A_H$	Low	$2A_H$	Forwarding Group 6 Outbound Port Map Low		rw	$FFFF_H$
$022B_H$	High	$2B_H$	Forwarding Group 6 Outbound Port Map High		rw	$3FF_H$

Table 15 EEPROM Format (cont'd)

Offset Hex		Index	Bit 15 - 8	Bit 7 - 0	Type	Default
$022C_H$	Low	$2C_H$	Forwarding Group 7 Outbound Port Map Low		rw	$FFFF_H$
$022D_H$	High	$2D_H$	Forwarding Group 7 Outbound Port Map High		rw	$3FF_H$
$022E_H$	Low	$2E_H$	Forwarding Group 8 Outbound Port Map Low		rw	$FFFF_H$
$022F_H$	High	$2F_H$	Forwarding Group 8 Outbound Port Map High		rw	$3FF_H$
0230_H	Low	30_H	Forwarding Group 9 Outbound Port Map Low		rw	$FFFF_H$
0231_H	High	31_H	Forwarding Group 9 Outbound Port Map High		rw	$3FF_H$
0232_H	Low	32_H	Forwarding Group 10 Outbound Port Map Low		rw	$FFFF_H$
0233_H	High	33_H	Forwarding Group 10 Outbound Port Map High		rw	$3FF_H$
0234_H	Low	34_H	Forwarding Group 11 Outbound Port Map Low		rw	$FFFF_H$
0235_H	High	35_H	Forwarding Group 11 Outbound Port Map High		rw	$3FF_H$
0236_H	Low	36_H	Forwarding Group 12 Outbound Port Map Low		rw	$FFFF_H$
0237_H	High	37_H	Forwarding Group 12 Outbound Port Map High		rw	$3FF_H$
0238_H	Low	38_H	Forwarding Group 13 Outbound Port Map Low		rw	$FFFF_H$
0239_H	High	39_H	Forwarding Group 13 Outbound Port Map High		rw	$3FF_H$
$023A_H$	Low	$3A_H$	Forwarding Group 14 Outbound Port Map Low		rw	$FFFF_H$
$023B_H$	High	$3B_H$	Forwarding Group 14 Outbound Port Map High		rw	$3FF_H$
$023C_H$	Low	$3C_H$	Forwarding Group 15 Outbound Port Map Low		rw	$FFFF_H$
$023D_H$	High	$3D_H$	Forwarding Group 15 Outbound Port Map High		rw	$3FF_H$
$023E_H$	Low	$3E_H$	Forwarding Group 16 Outbound Port Map Low		rw	$FFFF_H$
$023F_H$	High	$3F_H$	Forwarding Group 16 Outbound Port Map High		rw	$3FF_H$
0240_H	Low	40_H	Forwarding Group 17 Outbound Port Map Low		rw	$FFFF_H$
0241_H	High	41_H	Forwarding Group 17 Outbound Port Map High		rw	$3FF_H$
0242_H	Low	42_H	Forwarding Group 18 Outbound Port Map Low		rw	$FFFF_H$
0243_H	High	43_H	Forwarding Group 18 Outbound Port Map High		rw	$3FF_H$
0244_H	Low	44_H	Forwarding Group 19 Outbound Port Map Low		rw	$FFFF_H$
0245_H	High	45_H	Forwarding Group 19 Outbound Port Map High		rw	$3FF_H$
0246_H	Low	46_H	Forwarding Group 20 Outbound Port Map Low		rw	$FFFF_H$
0247_H	High	47_H	Forwarding Group 20 Outbound Port Map High		rw	$3FF_H$
0248_H	Low	48_H	Forwarding Group 21 Outbound Port Map Low		rw	$FFFF_H$
0249_H	High	49_H	Forwarding Group 21 Outbound Port Map High		rw	$3FF_H$
$024A_H$	Low	$4A_H$	Forwarding Group 22 Outbound Port Map Low		rw	$FFFF_H$
$024B_H$	High	$4B_H$	Forwarding Group 22 Outbound Port Map High		rw	$3FF_H$
$024C_H$	Low	$4C_H$	Forwarding Group 23 Outbound Port Map Low		rw	$FFFF_H$
$024D_H$	High	$4D_H$	Forwarding Group 23 Outbound Port Map High		rw	$3FF_H$
$024E_H$	Low	$4E_H$	Forwarding Group 24 Outbound Port Map Low		rw	$FFFF_H$
$024F_H$	High	$4F_H$	Forwarding Group 24 Outbound Port Map High		rw	$3FF_H$
0250_H	Low	50_H	Forwarding Group 25 Outbound Port Map Low		rw	$FFFF_H$
0251_H	High	51_H	Forwarding Group 25 Outbound Port Map High		rw	$3FF_H$
0252_H	Low	52_H	Forwarding Group 26 Outbound Port Map Low		rw	$FFFF_H$
0253_H	High	53_H	Forwarding Group 26 Outbound Port Map High		rw	$3FF_H$

Table 15 EEPROM Format (cont'd)

Offset Hex		Index	Bit 15 - 8	Bit 7 - 0	Type	Default
0254_H	Low	54_H	Forwarding Group 27 Outbound Port Map Low		rw	$FFFF_H$
0255_H	High	55_H	Forwarding Group 27 Outbound Port Map High		rw	$3FF_H$
0256_H	Low	56_H	Forwarding Group 28 Outbound Port Map Low		rw	$FFFF_H$
0257_H	High	57_H	Forwarding Group 28 Outbound Port Map High		rw	$3FF_H$
0258_H	Low	58_H	Forwarding Group 29 Outbound Port Map Low		rw	$FFFF_H$
0259_H	High	59_H	Forwarding Group 29 Outbound Port Map High		rw	$3FF_H$
$025A_H$	Low	$5A_H$	Forwarding Group 30 Outbound Port Map Low		rw	$FFFF_H$
$025B_H$	High	$5B_H$	Forwarding Group 30 Outbound Port Map High		rw	$3FF_H$
$025C_H$	Low	$5C_H$	Forwarding Group 31 Outbound Port Map Low		rw	$FFFF_H$
$025D_H$	High	$5D_H$	Forwarding Group 31 Outbound Port Map High		rw	$3FF_H$
$025E_H$	Low	$5E_H$	PVID shift	P0 VID	rw	1_H
$025F_H$	High	$5F_H$	P1 VID		rw	1_H
0260_H	Low	60_H	P2 VID		rw	1_H
0261_H	High	61_H	P3 VID		rw	1_H
0262_H	Low	62_H	P4 VID		rw	1_H
0263_H	High	63_H	P5 VID		rw	1_H
0264_H	Low	64_H	P6 VID		rw	1_H
0265_H	High	65_H	P7 VID		rw	1_H
0266_H	Low	66_H	P8 VID		rw	1_H
0267_H	High	67_H	P9 VID		rw	1_H
0268_H	Low	68_H	P10 VID		rw	1_H
0269_H	High	69_H	P11 VID		rw	1_H
$026A_H$	Low	$6A_H$	P12 VID		rw	1_H
$026B_H$	High	$6B_H$	P13 VID		rw	1_H
$026C_H$	Low	$6C_H$	P14 VID		rw	1_H
$026D_H$	High	$6D_H$	P15 VID		rw	1_H
$026E_H$	Low	$6E_H$	P16 VID		rw	1_H
$026F_H$	High	$6F_H$	P17 VID		rw	1_H
0270_H	Low	70_H	P18 VID		rw	1_H
0271_H	High	71_H	P19 VID		rw	1_H
0272_H	Low	72_H	P20 VID		rw	1_H
0273_H	High	73_H	P21 VID		rw	1_H
0274_H	Low	74_H	P22 VID		rw	1_H
0275_H	High	75_H	P23 VID		rw	1_H
0276_H	Low	76_H	P24 VID		rw	1_H
0277_H	High	77_H	P25 VID		rw	1_H
0278_H	Low	78_H	P0, P1, P2, P3 Bandwidth Control Register		rw	0_H
0279_H	High	79_H	P4, P5, P6, P7 Bandwidth Control Register		rw	0_H
$027A_H$	Low	$7A_H$	P8, P9, P10, P11 Bandwidth Control Register		rw	0_H
$027B_H$	High	$7B_H$	P12, P13, P14, P15 Bandwidth Control Register		rw	0_H

Table 15 EEPROM Format (cont'd)

Offset Hex		Index	Bit 15 - 8	Bit 7 - 0	Type	Default
$027C_H$	Low	$7C_H$	P16, P17, P18, P19 Bandwidth Control register		rw	0_H
$027D_H$	High	$7D_H$	P20, P21, P22, P23 Bandwidth Control Register		rw	0_H
$027E_H$	Low	$7E_H$	P25, P24 Bandwidth Control Register		rw	0_H
$027F_H$	High	$7F_H$	Bandwidth Control Enable Register Low		rw	0_H
0280_H	Low	80_H	Bandwidth Control Enable Register High		rw	0_H
0281_H	High	81_H	Reserved		rw	0_H
0282_H	Low	82_H	Reserved		rw	0_H
0283_H	High	83_H	Reserved		rw	100_H
0284_H	Low	84_H	Reserved		rw	0_H
0285_H	High	85_H	Reserved		rw	0_H
0286_H	Low	86_H	Reserved		rw	0_H
0287_H	High	87_H	Reserved		rw	0_H
0288_H	Low	88_H	Reserved		rw	0_H
0289_H	High	89_H	Reserved		rw	0_H
$028A_H$	Low	$8A_H$	Reserved		rw	$FF00_H$
$028B_H$	HIGH	$8B_H$	Customized PHY Control Group 0		rw	0_H
$028C_H$	Low	$8C_H$	Customized PHY Control Group 1		rw	0_H
$028D_H$	HIGH	$8D_H$	Customized PHY Control Group 2		rw	0_H
$028E_H$	Low	$8E_H$	Customized PHY Control Group 3		rw	0_H
$028F_H$	HIGH	$8F_H$	Group 0 PHY Customized DATA 0		rw	0_H
0290_H	Low	90_H	Group 0 PHY Customized DATA 1		rw	0_H
0291_H	HIGH	91_H	Group 1 PHY Customized DATA 0		rw	0_H
0292_H	Low	92_H	Group 1 PHY Customized DATA 1		rw	0_H
0293_H	HIGH	93_H	Group 2 PHY Customized DATA 0		rw	0_H
0294_H	Low	94_H	Group 2 PHY Customized DATA 1		rw	0_H
0295_H	HIGH	95_H	Group 3 PHY Customized DATA 0		rw	0_H
0296_H	Low	96_H	Group 3 PHY Customized DATA 1		rw	0_H
0297_H	HIGH	97_H	PHY Customized Enable Register		rw	0_H
0298_H	Low	98_H	PPPOE Control Register 0		rw	0_H
0299_H	HIGH	99_H	PPPOE Control Register 1		rw	0_H
$029A_H$	Low	$9A_H$	PHY Control Register 0		rw	0_H
$029B_H$	HIGH	$9B_H$	PHY Control Register 1		rw	0_H
$029C_H$	Low	$9C_H$	Disable MDIO Active Register 0		rw	0_H
$029D_H$	HIGH	$9D_H$	Disable MDIO Active Register 1		rw	0_H
$029E_H$	Low	$9E_H$	Disable Port Register 0		rw	0_H
$029F_H$	HIGH	$9F_H$	Disable Port Register 1		rw	0_H
$02A0_H$	Low	$A0_H$	IGMP Enable Register 0		rw	0_H
$02A1_H$	HIGH	$A1_H$	IGMP Enable Register 1		rw	0_H
$02A2_H$	Low	$A2_H$	CPU Control Register		rw	$001F_H$
$02A3_H$	HIGH	$A3_H$	MAC Forward Mode Register 0		rw	4_H

Table 15 EEPROM Format (cont'd)

Offset Hex		Index	Bit 15 - 8	Bit 7 - 0	Type	Default
$02A4_H$	Low	$A4_H$	MAC Forward Mode Register 1		rw	3_H
$02A5_H$	HIGH	$A5_H$	MAC Forward Mode Register 2		rw	0_H
$02A6_H$	Low	$A6_H$	Trunking Enable Register 0		rw	0_H
$02A7_H$	HIGH	$A7_H$	Trunking Enable Register 1		rw	0_H

3.2.1 EEPROM Registers Overview

Table 16 Registers Address Space

Module	Base Address	End Address	Note
EEPROM	0200_H	$02A7_H$	

Table 17 Registers Overview

Register Short Name	Register Long Name	Offset Address	Page Number
SIG	Signature	0200_H	42
GCR	Global Configuration Register	0201_H	42
PCR_0	Port 0 Configuration Register	0202_H	44
PCR_1	Port 1 Configuration	0203_H	47
PCR_2	Port 2 Configuration	0204_H	47
PCR_3	Port 3 Configuration	0205_H	47
PCR_4	Port 4 Configuration	0206_H	47
PCR_5	Port 5 Configuration	0207_H	47
PCR_6	Port 6 Configuration	0208_H	47
PCR_7	Port 7 Configuration	0209_H	47
PCR_8	Port 8 Configuration	$020A_H$	47
PCR_9	Port 9 Configuration	$020B_H$	47
PCR_10	Port 10 Configuration	$020C_H$	47
PCR_11	Port 11 Configuration	$020D_H$	47
PCR_12	Port 12 Configuration	$020E_H$	47
PCR_13	Port 13 Configuration	$020F_H$	47
PCR_14	Port 14 Configuration	0210_H	47
PCR_15	Port 15 Configuration	0211_H	47
PCR_16	Port 16 Configuration	0212_H	47
PCR_17	Port 17 Configuration	0213_H	47
PCR_18	Port 18 Configuration	0214_H	47
PCR_19	Port 19 Configuration	0215_H	47
PCR_20	Port 20 Configuration	0216_H	47
PCR_21	Port 21 Configuration	0217_H	47
PCR_22	Port 22 Configuration	0218_H	47
PCR_23	Port 23 Configuration	0219_H	47
PCR_24	Port 24 Configuration	$021A_H$	47
PCR_25	Port 25 Configuration	$021B_H$	47
MC	Miscellaneous Configuration	$021C_H$	48
VLAN	VLAN(TOS) Priority Map	$021D_H$	48
FGOPML_0	Forwarding Group 0 Outbound Port Map Low	$021E_H$	50
FGOPMH_0	Forwarding Group 0 Outbound Port Map High	$021F_H$	52
FGOPML_1	Forwarding Group 1 Outbound Port Map Low	0220_H	51
FGOPMH_1	Forwarding Group 1 Outbound Port Map High	0221_H	53

Table 17 Registers Overview (cont'd)

Register Short Name	Register Long Name	Offset Address	Page Number
FGOPML_2	Forwarding Group 2 Outbound Port Map Low	0222_H	51
FGOPMH_2	Forwarding Group 2 Outbound Port Map High	0223_H	53
FGOPML_3	Forwarding Group 3 Outbound Port Map Low	0224_H	51
FGOPMH_3	Forwarding Group 3 Outbound Port Map High	0225_H	53
FGOPML_4	Forwarding Group 4 Outbound Port Map Low	0226_H	51
FGOPMH_4	Forwarding Group 4 Outbound Port Map High	0227_H	53
FGOPML_5	Forwarding Group 5 Outbound Port Map Low	0228_H	51
FGOPMH_5	Forwarding Group 5 Outbound Port Map High	0229_H	53
FGOPML_6	Forwarding Group 6 Outbound Port Map Low	$022A_H$	51
FGOPMH_6	Forwarding Group 6 Outbound Port Map High	$022B_H$	53
FGOPML_7	Forwarding Group 7 Outbound Port Map Low	$022C_H$	51
FGOPMH_7	Forwarding Group 7 Outbound Port Map High	$022D_H$	53
FGOPML_8	Forwarding Group 8 Outbound Port Map Low	$022E_H$	51
FGOPMH_8	Forwarding Group 8 Outbound Port Map High	$022F_H$	53
FGOPML_9	Forwarding Group 9 Outbound Port Map Low	0230_H	51
FGOPMH_9	Forwarding Group 9 Outbound Port Map High	0231_H	53
FGOPML_10	Forwarding Group 10 Outbound Port Map Low	0232_H	51
FGOPMH_10	Forwarding Group 10 Outbound Port Map High	0233_H	53
FGOPML_11	Forwarding Group 11 Outbound Port Map Low	0234_H	51
FGOPMH_11	Forwarding Group 11 Outbound Port Map High	0235_H	53
FGOPML_12	Forwarding Group 12 Outbound Port Map Low	0236_H	51
FGOPMH_12	Forwarding Group 12 Outbound Port Map High	0237_H	53
FGOPML_13	Forwarding Group 13 Outbound Port Map Low	0238_H	51
FGOPMH_13	Forwarding Group 13 Outbound Port Map High	0239_H	53
FGOPML_14	Forwarding Group 14 Outbound Port Map Low	$023A_H$	51
FGOPMH_14	Forwarding Group 14 Outbound Port Map High	$023B_H$	53
FGOPML_15	Forwarding Group 15 Outbound Port Map Low	$023C_H$	51
FGOPMH_15	Forwarding Group 15 Outbound Port Map High	$023D_H$	53
FGOPML_16	Forwarding Group 16 Outbound Port Map Low	$023E_H$	51
FGOPMH_16	Forwarding Group 16 Outbound Port Map High	$023F_H$	53
FGOPML_17	Forwarding Group 17 Outbound Port Map Low	0240_H	51
FGOPMH_17	Forwarding Group 17 Outbound Port Map High	0241_H	53
FGOPML_18	Forwarding Group 18 Outbound Port Map Low	0242_H	52
FGOPMH_18	Forwarding Group 18 Outbound Port Map High	0243_H	53
FGOPML_19	Forwarding Group 19 Outbound Port Map Low	0244_H	52
FGOPMH_19	Forwarding Group 19 Outbound Port Map High	0245_H	53
FGOPML_20	Forwarding Group 20 Outbound Port Map Low	0246_H	52
FGOPMH_20	Forwarding Group 20 Outbound Port Map High	0247_H	53
FGOPML_21	Forwarding Group 21 Outbound Port Map Low	0248_H	52
FGOPMH_21	Forwarding Group 21 Outbound Port Map High	0249_H	53
FGOPML_22	Forwarding Group 22 Outbound Port Map Low	$024A_H$	52

Table 17 Registers Overview (cont'd)

Register Short Name	Register Long Name	Offset Address	Page Number
FGOPMH_22	Forwarding Group 22 Outbound Port Map High	$024B_H$	53
FGOPML_23	Forwarding Group 23 Outbound Port Map Low	$024C_H$	52
FGOPMH_23	Forwarding Group 23 Outbound Port Map High	$024D_H$	54
FGOPML_24	Forwarding Group 24 Outbound Port Map Low	$024E_H$	52
FGOPMH_24	Forwarding Group 24 Outbound Port Map High	$024F_H$	54
FGOPML_25	Forwarding Group 25 Outbound Port Map Low	0250_H	52
FGOPMH_25	Forwarding Group 25 Outbound Port Map High	0251_H	54
FGOPML_26	Forwarding Group 26 Outbound Port Map Low	0252_H	52
FGOPMH_26	Forwarding Group 26 Outbound Port Map High	0253_H	54
FGOPML_27	Forwarding Group 27 Outbound Port Map Low	0254_H	52
FGOPMH_27	Forwarding Group 27 Outbound Port Map High	0255_H	54
FGOPML_28	Forwarding Group 28 Outbound Port Map Low	0256_H	52
FGOPMH_28	Forwarding Group 28 Outbound Port Map High	0257_H	54
FGOPML_29	Forwarding Group 29 Outbound Port Map Low	0258_H	52
FGOPMH_29	Forwarding Group 29 Outbound Port Map High	0259_H	54
FGOPML_30	Forwarding Group 30 Outbound Port Map Low	$025A_H$	52
FGOPMH_30	Forwarding Group 30 Outbound Port Map High	$025B_H$	54
FGOPML_31	Forwarding Group 31 Outbound Port Map Low	$025C_H$	52
FGOPMH_31	Forwarding Group 31 Outbound Port Map High	$025D_H$	54
P0VIDS	P0 VID and PVID Shift	$025E_H$	54
P1_VID	P1 VID Configuration	$025F_H$	55
P2_VID	P2 VID Configuration	0260_H	56
P3_VID	P3 VID Configuration	0261_H	56
P4_VID	P4 VID Configuration	0262_H	56
P5_VID	P5 VID Configuration	0263_H	56
P6_VID	P6 VID Configuration	0264_H	56
P7_VID	P7 VID Configuration	0265_H	56
P8_VID	P8 VID Configuration	0266_H	56
P9_VID	P9 VID Configuration	0267_H	56
P10_VID	P10 VID Configuration	0268_H	56
P11_VID	P11 VID Configuration	0269_H	56
P12_VID	P12 VID Configuration	$026A_H$	56
P13_VID	P13 VID Configuration	$026B_H$	56
P14_VID	P14 VID Configuration	$026C_H$	56
P15_VID	P15 VID Configuration	$026D_H$	56
P16_VID	P16 VID Configuration	$026E_H$	56
P17_VID	P17 VID Configuration	$026F_H$	56
P18_VID	P18 VID Configuration	0270_H	56
P19_VID	P19 VID Configuration	0271_H	56
P20_VID	P20 VID Configuration	0272_H	56
P21_VID	P21 VID Configuration	0273_H	56

Table 17 Registers Overview (cont'd)

Register Short Name	Register Long Name	Offset Address	Page Number
P22_VID	P22 VID Configuration	0274_H	56
P23_VID	P23 VID Configuration	0275_H	56
P24_VID	P24 VID Configuration	0276_H	56
P25_VID	P25 VID Configuration	0277_H	56
P0_3_BCR	P0, P1, P2, P3 Bandwidth Control Register	0278_H	56
P4_7_BCR	P4, P5, P6, P7 Bandwidth Control Register	0279_H	58
P8_11_BCR	P8, P9, P10, P11 Bandwidth Control Register	$027A_H$	59
P12_15_BCR	P12, P13, P14, P15 Bandwidth Control Register	$027B_H$	60
P16_19_BCR	P16, P17, P18, P19 Bandwidth Control Register	$027C_H$	61
P20_23_BCR	P20, P21, P22, P23 Bandwidth Control Register	$027D_H$	63
P24_25_BCR	P24, P25 Bandwidth Control Register	$027E_H$	64
BCERL	Bandwidth Control Enable Register Low	$027F_H$	65
BCERH	Bandwidth Control Enable Register High	0280_H	66
RES1	Reserved Register 1	0281_H	66
RES2	Reserved Register 2	0282_H	67
RES3	Reserved Register 3	0283_H	67
RES4	Reserved Register 4	0284_H	67
RES5	Reserved Register 5	0285_H	67
RES6	Reserved Register 6	0286_H	67
RES7	Reserved Register 7	0287_H	67
RES8	Reserved Register 8	0288_H	67
RES9	Reserved Register 9	0289_H	67
RES10	Reserved Register 10	$028A_H$	67
CPHYCG0	Customized PHY Control Group 0	$028B_H$	67
CPHYCG1	Customized PHY Control Group 1	$028C_H$	68
CPHYCG2	Customized PHY Control Group 2	$028D_H$	69
CPHYCG3	Customized PHY Control Group 3	$028E_H$	70
G0PHYCD0	Group 0 PHY Customized DATA 0	$028F_H$	71
G0PHYCD1	Group 0 PHY Customized DATA 1	0290_H	71
G1PHYCD0	Group 1 PHY Customized DATA 0	0291_H	72
G1PHYCD1	Group 1 PHY Customized DATA 1	0292_H	72
G2PHYCD0	Group 2 PHY Customized DATA 0	0293_H	72
G2PHYCD1	Group 2 PHY Customized DATA 1	0294_H	73
G3PHYCD0	Group 3 PHY Customized DATA 0	0295_H	73
G3PHYCD1	Group 3 PHY Customized DATA 1	0296_H	73
PHYCE	PHY Customized Enable Register	0297_H	74
PPPOEC0	PPPOE Control Register 0	0298_H	75
PPPOEC1	PPPOE Control Register 1	0299_H	76
PHYCR0	PHY Control Register 0	$029A_H$	76
PHYCR1	PHY Control Register 1	$029B_H$	78
DMDIOAR0	Disable MDIO Active Register 0	$029C_H$	79

Table 17 Registers Overview (cont'd)

Register Short Name	Register Long Name	Offset Address	Page Number
DMDIOAR1	Disable MDIO Active Register 1	$029D_H$	80
PDR0	Port Disable Register 0	$029E_H$	80
PDR1	Port Disable Register 1	$029F_H$	81
IGMPSCR0	IGMP Snooping Control Register 0	$02A0_H$	82
IGMPSCR1	IGMP Snooping Control Register 1	$02A1_H$	83
CPUCR	CPU Control Register	$02A2_H$	83
SMACFCR0	Special MAC Forward Control Register 0	$02A3_H$	85
SMACFCR1	Special MAC Forward Control Register 1	$02A4_H$	86
SMACFCR2	Special MAC Forward Control Register 2	$02A5_H$	87
TER0	Trunking Enable Register 0	$02A6_H$	88
TER1	Trunking Enable Register 1	$02A7_H$	89

The register is addressed wordwise.

Table 18 Register Access Types

Mode	Symbol	Description HW	Description SW
read/write	rw	Register is used as input for the HW	Register is read and writable by SW
read	r	Register is written by HW (register between input and output -> one cycle delay)	Value written by software is ignored by hardware; that is, software may write any value to this field without affecting hardware behavior (= Target for development.)
Read only	ro	Register is set by HW (register between input and output -> one cycle delay)	SW can only read this register
Read virtual	rv	Physically, there is no new register, the input of the signal is connected directly to the address multiplexer.	SW can only read this register
Latch high, self clearing	lhsc	Latch high signal at high level, clear on read	SW can read the register
Latch low, self clearing	llsc	Latch high signal at low-level, clear on read	SW can read the register
Latch high, mask clearing	lhmk	Latch high signal at high level, register cleared with written mask	SW can read the register, with write mask the register can be cleared (1 clears)
Latch low, mask clearing	llmk	Latch high signal at low-level, register cleared on read	SW can read the register, with write mask the register can be cleared (1 clears)
Interrupt high, self clearing	ihsc	Differentiate the input signal (low->high) register cleared on read	SW can read the register
Interrupt low, self clearing	ilsc	Differentiate the input signal (high->low) register cleared on read	SW can read the register
Interrupt high, mask clearing	ihmk	Differentiate the input signal (high->low) register cleared with written mask	SW can read the register, with write mask the register can be cleared
Interrupt low, mask clearing	ilmk	Differentiate the input signal (low->high) register cleared with written mask	SW can read the register, with write mask the register can be cleared

Table 18 Register Access Types (cont'd)

Mode	Symbol	Description HW	Description SW
Interrupt enable register	ien	Enables the interrupt source for interrupt generation	SW can read and write this register
latch_on_reset	lor	rw register, value is latched after first clock cycle after reset	Register is read and writable by SW
Read/write self clearing	rwsc	Register is used as input for the hw, the register will be cleared due to a HW mechanism.	Writing to the register generates a strobe signal for the HW (1 pdi clock cycle) Register is read and writable by SW.

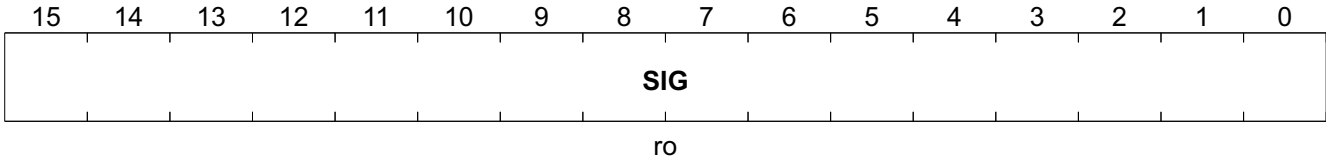
Table 19 Registers Clock DomainsRegisters Clock Domains

Clock Short Name	Description

3.2.1.1

Signature

SIG	Offset	Reset Value
Signature	0200_H	4154_H



Field	Bits	Type	Description
SIG	15:0	ro	**Signature** The value must be at 4154_H. ADM6926/X uses this value to check if the EEPROM is attached. If the value in the EEPROM doesn't equal to 4154_H, the ADM6926/X will not load the EEPROM even if the EEPROM is attached.

Global Configuration Register

GCR	Offset	Reset Value
Global Configuration Register	0201_H	3800_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res	FMCE	LEB	FNTM	BM	VGM	CVG	DM				PQR		BSFE	BST	
	rw	rw	rw	rw	rw	rw	rw				rw		rw	rw	

Field	Bits	Type	Description
FMCE	14	rw	**Fast Management Clock Enable Bit** 0_B , The switch will use 2.5 M clock to configure the phys. 1_B , The switch will use 10 M clock to configure the phys.
LEB	13	rw	**Length 1536 Enable Bit** 0_B , The switch can receive packets of less then 1518 bytes. 1_B , The switch can receive packets of less than 1536 bytes.
FNTM	12	rw	**Force No Tag Mode** 0_B , The switch is not configured to Force No Tag Mode. 1_B , The switch is configured to Force No Tag Mode. In this mode, the ADM6926/X will not recognize the VLAN TAG even if they contain a Tag Header.
BM	11	rw	**Bypass Mode** 0_B , The switch is not configured to Bypass Mode. 1_B , The switch is configured to Bypass Mode. The packets will not be modified when they are transmitted.
VGM	10	rw	**VLAN Group Mode** 1_B , The switch is configured to Tagged Based VLAN 0_B , The switch is configured to Port Based VLAN.
CVG	9	rw	**Check VLAN Group** 0_B , The ADM6926/X will disable the Check VLAN Group function. 1_B , The ADM6926/X will check if the packets and the receiving port are at the same Forwarding Group. That is, the output port map for the receiving packet must contain the receiving port. If they belong to different Forwarding Group, the receiving packets will be discarded. *Note: Example: Port 3 receives a packet and finds Forwarding Group contains P0, P1, and P2 (doesn't contain P3). This packet will be dropped.*
DM	8:5	rw	**Discard Mode** This function enables the switch to discard packets according to their priorities if the receiving port disables the flow control function. Users could use this to prevent packets with the low priority to block those with high priority. Bit[8:7] = High Queue Discard Mode (see Sec. 3.1.18) Bit[6:5] = Low Queue Discard Mode

Field	Bits	Type	Description
PQR	4:3	rw	**Priority Queue Ratio** The ADM6926/X supports two priorities on each output port using weighted round robin scheme. The ratio between the low and high queue is as follows: Bit[4:3] Ratio 00_B , 1:2 01_B , 1:4 10_B , 1:8 11_B , 1:16
BSFE	2	rw	**Broadcast Storm Filtering Enable Bit** 0_B , The ADM6926/X disables the broadcast storm filtering function. 1_B , The ADM6926/X enables the broadcast storm filtering function.
BST	1:0	rw	**Broadcast Storm Threshold**

Port 0 Configuration Register

PCR_0	Offset	Reset Value
Port 0 Configuration Register	0202_H	$80FF_H$

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BPEB	FSM		PPM	EPP	TVP	SFE	TP	DA	SA	ANE	FCA	100FDA	100HDA	10FDA	10HDA
rw	rw		rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
BPEB	15	rw	**Back Pressure Enable Bit** 0_B , The MAC controller doesn't support back-pressure function in half duplex. 1_B , The MAC controller supports back-pressure function in half duplex.

Field	Bits	Type	Description
FSM	14:13	rw	**Four Security Mode** 00_B , The switch will forward packets with “unknown source addresses” to the CPU port and not learn it if the receiving port is configured to enable security function. The “unknown source address” means that we can’t find an equal address existed in the learning table and its corresponding port number equals to the receiving port. This function needs CUP’s help because we need to create a “static address” to the learning table from the CPU. “Static” means this address will always exist in the leaning table and can only be removed through the CPU. When the address is configured to “Static”, we can prevent this address from overlapping when it is received from a port without the security function enabled. 01_B , The switch will discard packets with “unknown source addresses” and not learn it if the receiving port is configured to enable security function. Only packets with source addresses existed in the learning table will be forwarded. 10_B , The first received packets will be locked at the receiving port if the receiving port is configured to enable security function. Only the packets with the source address same as the locked one will be forwarded and learned. 11_B , The first received packets will be locked as above. The difference is that the receiving port will not receive and learn packets any more after the link goes down even it links up again (it may happen if the station moves to the other port).
PPM	12	rw	**Port-base Priority Mapping** 0_B , Mapped for the Low Queue. 1_B , Mapped for the High Queue.
EPP	11	rw	**Enable Port-base Priority** 0_B , The switch will use the IPv4 or Tag priority fields for the queue mapping (See Bit [10]). If the packets contain no priority field, then the switch will use the Port-Priority for the default priority. 1_B , The switch will always use the Port-Priority for the queue mapping even if the receiving packets contain IPv4 or Tag information.
TVP	10	rw	**TOS over VLAN Priority** 0_B , When the receiving packets contain the IPv4 and Tag Priority at the same time, the switch will use Tag priority field for the queue mapping. 1_B , When the receiving packets contain the IPv4 and Tag Priority at the same time, the switch will use IPv4 priority field for the queue mapping.
SFE	9	rw	**Security Function Enable** 0_B , The switch disables the security function. 1_B , The switch enables the security function. Four security modes could be selected through Bit[14:13].

Field	Bits	Type	Description
TP	8	rw	**Tagged Port** 0_B , The transmitted port is configured to an untagged port. The transmitted packets from an untagged port will not contain a Tag Header except the transmitted packets are management packet or the Bypass Mode is enabled. 1_B , The transmitted port is configured to a tagged port. The transmitted packets from a tagged port will always contain a Tag Header except the transmitted packets are management packet or the Bypass Mode is enabled.
DA	7	rw	**Duplex Ability** This bit will be used as Bit 8 (Duplex Select) in the Basic Mode Control Register if bypass management function is not enabled, and be used as Duplex Desired if bypass management function is enabled. 0_B , Half Duplex Enabled. 1_B , Full Duplex Enabled.
SA	6	rw	**Speed Ability** This bit will be used as Bit 13 (Speed Select) in the Basic Mode Control Register if bypass management function is not enabled, and be used as Speed Desired if bypass management function is enabled. 0_B , 10 Mbit/s Enabled. 1_B , 100 Mbit/s Enabled.
ANE	5	rw	**Auto Negotiation Enable in Basic Mode Control Register** 0_B , Auto-Negotiation is Disabled. 1_B , Auto-Negotiation is Enabled.
FCA	4	rw	**802.3x Flow Control Ability in Full Duplex** 0_B , (1). Mac controller doesn't support Pause Frames when the port is configured to bypass management function from MDC/MDIO. (2). If the port is not configured to bypass management function form MDC/MDIO, then it will be used as the Pause bit in Auto-Negotiation Advertisement Register and the Pause function will not be advertised. If Auto-Negotiation function is disabled, then this bit is used and Pause is not supported. (3). If the port is not configured to bypass management function from MDC/MDIO and no PHY is attached to this port, the MAC controller will not support Pause Frames in the full duplex. 1_B , (1). MAC controller supports Pause Frames when the port is configured to bypass management function from MDC/MDIO. (2). If the port is not configured to bypass management function form MDC/MDIO, then it will be used as the Pause bit in Auto-Negotiation Advertisement Register and the Pause function will be advertised. If Auto-Negotiation function is disabled, then this bit is used and Pause is supported. (3). If the port is not configured to bypass management function from MDC/MDIO and no PHY is attached to this port, the MAC controller will support Pause Frames in the full duplex.
100FDA	3	rw	**100Base-TX Full Duplex Ability in Auto-Negotiation Advertisement Register** 0_B , 100Base-Tx Full Duplex is not advertised. 1_B , 100Base-TX Full Duplex is advertised.

Field	Bits	Type	Description
100HDA	2	rw	**100Base-TX Half Duplex Ability in Auto-Negotiation Advertisement Register** 0_B , 100Base-TX Half Duplex is not advertised. 1_B , 100Base-TX Half Duplex is advertised.
10FDA	1	rw	**10Base-T Full Duplex Ability in Auto-Negotiation Advertisement Register** 0_B , 10Base-T Full Duplex is not advertised. 1_B , 10Base-T Full Duplex is advertised.
10HDA	0	rw	**10Base-T Half Duplex Ability in Auto-Negotiation Advertisement Register** 0_B , 10Base-T Half Duplex is not advertised. 1_B , 10Base-T Half Duplex is advertised.

All PCR_x registers have the same structure and characteristics, see **PCR_0**.
The offset addresses of the other PCR_x registers are listed in **Table 20**.

Table 20 PCR_x Registers

Register Short Name	Register Long Name	Offset Address	Page Number
PCR_1	Port 1 Configuration	0203_H	
PCR_2	Port 2 Configuration	0204_H	
PCR_3	Port 3 Configuration	0205_H	
PCR_4	Port 4 Configuration	0206_H	
PCR_5	Port 5 Configuration	0207_H	
PCR_6	Port 6 Configuration	0208_H	
PCR_7	Port 7 Configuration	0209_H	
PCR_8	Port 8 Configuration	$020A_H$	
PCR_9	Port 9 Configuration	$020B_H$	
PCR_10	Port 10 Configuration	$020C_H$	
PCR_11	Port 11 Configuration	$020D_H$	
PCR_12	Port 12 Configuration	$020E_H$	
PCR_13	Port 13 Configuration	$020F_H$	
PCR_14	Port 14 Configuration	0210_H	
PCR_15	Port 15 Configuration	0211_H	
PCR_16	Port 16 Configuration	0212_H	
PCR_17	Port 17 Configuration	0213_H	
PCR_18	Port 18 Configuration	0214_H	
PCR_19	Port 19 Configuration	0215_H	
PCR_20	Port 20 Configuration	0216_H	
PCR_21	Port 21 Configuration	0217_H	
PCR_22	Port 22 Configuration	0218_H	
PCR_23	Port 23 Configuration	0219_H	
PCR_24	Port 24 Configuration	$021A_H$	
PCR_25	Port 25 Configuration	$021B_H$	

Miscellaneous Configuration

MC	Offset	Reset Value
Miscellaneous Configuration	$021C_H$	0820_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res		Res				CLEDE	Res					ERID	Res	RCD	DBF
		ro				rw	ro					rw	ro	rw	rw

Field	Bits	Type	Description
Res	13:10	ro	**Reserved**
CLEDE	9	rw	**Collision LED Enable** 0_B , The switch will not provide two collision LEDs for 10M and 100M domain individually 1_B , The switch will provide two collision LEDs for 10M and 100M domain individually and flash in rate of 2 Hz.
Res	8:4	ro	**Reserved**
ERID	3	rw	**Enable Replace VLAN ID** 0_B , The switch will use the original VID received from the Tag Header. 1_B , The switch will replace the VID with the PVID associated with the receiving port when the received packets are priority tagged or its VID in the Tag Header equals to 1.
Res	2	ro	**Reserved**
RCD	1	rw	**Recommend 16th Collision Drop** 0_B , The Mac controller will retransmit packets even when the collision count is larger than 16. 1_B , The Mac controller will drop packets when the collision count is larger than 16.
DBF	0	rw	**Disable CSMA/CD Back-off Function** 0_B , The Mac controller supports random back off function. 1_B , The MAC controller will disable random back off function.

VLAN(TOS) Priority Map

VLAN	Offset	Reset Value
VLAN(TOS) Priority Map	$021D_H$	0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MPQ7	MPQ6	MPQ5	MPQ4	MPQ3	MPQ2	MPQ1	MPQ0	MPQT7	MPQT6	MPQT5	MPQT4	MPQT3	MPQT2	MPQT1	MPQT0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
MPQ7	15	rw	**Mapped Priority Queue of TOS 7** 0_B , Mapped for Low Queue 1_B , Mapped for High Queue
MPQ6	14	rw	**Mapped Priority Queue of TOS 6** 0_B , Mapped for Low Queue 1_B , Mapped for High Queue
MPQ5	13	rw	**Mapped Priority Queue of TOS 5** 0_B , Mapped for Low Queue 1_B , Mapped for High Queue
MPQ4	12	rw	**Mapped Priority Queue of TOS 4** 0_B , Mapped for Low Queue 1_B , Mapped for High Queue
MPQ3	11	rw	**Mapped Priority Queue of TOS 3** 0_B , Mapped for Low Queue 1_B , Mapped for High Queue
MPQ2	10	rw	**Mapped Priority Queue of TOS 2** 0_B , Mapped for Low Queue 1_B , Mapped for High Queue
MPQ1	9	rw	**Mapped Priority Queue of TOS 1** 0_B , Mapped for Low Queue 1_B , Mapped for High Queue
MPQ0	8	rw	**Mapped Priority Queue of TOS 0** 0_B , Mapped for Low Queue 1_B , Mapped for High Queue
MPQT7	7	rw	**Mapped Priority Queue of Tag Value 7** 0_B , Mapped for Low Queue 1_B , Mapped for High Queue
MPQT6	6	rw	**Mapped Priority Queue of Tag Value 6** 0_B , Mapped for Low Queue 1_B , Mapped for High Queue
MPQT5	5	rw	**Mapped Priority Queue of Tag Value 5** 0_B , Mapped for Low Queue 1_B , Mapped for High Queue
MPQT4	4	rw	**Mapped Priority Queue of Tag Value 4** 0_B , Mapped for Low Queue 1_B , Mapped for High Queue
MPQT3	3	rw	**Mapped Priority Queue of Tag Value 3** 0_B , Mapped for Low Queue 1_B , Mapped for High Queue
MPQT2	2	rw	**Mapped priority Queue of Tag Value 2** 0_B , Mapped for Low Queue 1_B , Mapped for High Queue
MPQT1	1	rw	**Mapped Priority Queue of Tag Value 1** 0_B , Mapped for Low Queue 1_B , Mapped for High Queue

Field	Bits	Type	Description
MPQT0	0	rw	**Mapped Priority Queue of Tag Value 0** 0_B , Mapped for Low Queue 1_B , Mapped for High Queue

Forwarding Group 0 Outbound Port Map Low

FGOPML_0 **Offset** **Reset Value**
Forwarding Group 0 Outbound Port Map Low **$021E_H$** **$FFFF_H$**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FG15	**FG14**	**FG13**	**FG12**	**FG11**	**FG10**	**FG9**	**FG8**	**FG7**	**FG6**	**FG5**	**FG4**	**FG3**	**FG2**	**FG1**	**FG0**
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
FG15	15	rw	**Forwarding Group Port 15** 0_B , Port 15 is not in the Forwarding Group 1_B , Port 15 is in the Forwarding Group
FG14	14	rw	**Forwarding Group Port 14** 0_B , Port 14 is not in the Forwarding Group 1_B , Port 14 is in the Forwarding Group
FG13	13	rw	**Forwarding Group Port 13** 0_B , Port 13 is not in the Forwarding Group 1_B , Port 13 is in the Forwarding Group
FG12	12	rw	**Forwarding Group Port 12** 0_B , Port 12 is not in the Forwarding Group 1_B , Port 12 is in the Forwarding Group
FG11	11	rw	**Forwarding Group Port 11** 0_B , Port 11 is not in the Forwarding Group 1_B , Port 11 is in the Forwarding Group
FG10	10	rw	**Forwarding Group Port 10** 0_B , Port 10 is not in the Forwarding Group 1_B , Port 10 is in the Forwarding Group
FG9	9	rw	**Forwarding Group Port 9** 0_B , Port 9 is not in the Forwarding Group 1_B , Port 9 is in the Forwarding Group
FG8	8	rw	**Forwarding Group Port 8** 0_B , Port 8 is not in the Forwarding Group 1_B , Port 8 is in the Forwarding Group
FG7	7	rw	**Forwarding Group Port 7** 0_B , Port 7 is not in the Forwarding Group 1_B , Port 7 is in the Forwarding Group

Field	Bits	Type	Description
FG6	6	rw	**Forwarding Group Port 6** 0_B , Port 6 is not in the Forwarding Group 1_B , Port 6 is in the Forwarding Group
FG5	5	rw	**Forwarding Group Port 5** 0_B , Port 5 is not in the Forwarding Group 1_B , Port 5 is in the Forwarding Group
FG4	4	rw	**Forwarding Group Port 4** 0_B , Port 4 is not in the Forwarding Group 1_B , Port 4 is in the Forwarding Group
FG3	3	rw	**Forwarding Group Port 3** 0_B , Port 3 is not in the Forwarding Group 1_B , Port 3 is in the Forwarding Group
FG2	2	rw	**Forwarding Group Port 2** 0_B , Port 2 is not in the Forwarding Group 1_B , Port 2 is in the Forwarding Group
FG1	1	rw	**Forwarding Group Port 1** 0_B , Port 1 is not in the Forwarding Group 1_B , Port 1 is in the Forwarding Group
FG0	0	rw	**Forwarding Group Port 0** 0_B , Port 0 is not in the Forwarding Group 1_B , Port 0 is in the Forwarding Group

All FGOPML_x registers have the same structure and characteristics, see **FGOPML_0**. The offset addresses of the other FGOPML_x registers are listed in **Table 21**.

Table 21 FGOPML_x Registers

Register Short Name	Register Long Name	Offset Address	Page Number
FGOPML_1	Forwarding Group 1 Outbound Port Map Low	0220_H	
FGOPML_2	Forwarding Group 2 Outbound Port Map Low	0222_H	
FGOPML_3	Forwarding Group 3 Outbound Port Map Low	0224_H	
FGOPML_4	Forwarding Group 4 Outbound Port Map Low	0226_H	
FGOPML_5	Forwarding Group 5 Outbound Port Map Low	0228_H	
FGOPML_6	Forwarding Group 6 Outbound Port Map Low	$022A_H$	
FGOPML_7	Forwarding Group 7 Outbound Port Map Low	$022C_H$	
FGOPML_8	Forwarding Group 8 Outbound Port Map Low	$022E_H$	
FGOPML_9	Forwarding Group 9 Outbound Port Map Low	0230_H	
FGOPML_10	Forwarding Group 10 Outbound Port Map Low	0232_H	
FGOPML_11	Forwarding Group 11 Outbound Port Map Low	0234_H	
FGOPML_12	Forwarding Group 12 Outbound Port Map Low	0236_H	
FGOPML_13	Forwarding Group 13 Outbound Port Map Low	0238_H	
FGOPML_14	Forwarding Group 14 Outbound Port Map Low	$023A_H$	
FGOPML_15	Forwarding Group 15 Outbound Port Map Low	$023C_H$	
FGOPML_16	Forwarding Group 16 Outbound Port Map Low	$023E_H$	
FGOPML_17	Forwarding Group 17 Outbound Port Map Low	0240_H	

Table 21 FGOPML_x Registers (cont'd)

Register Short Name	Register Long Name	Offset Address	Page Number
FGOPML_18	Forwarding Group 18 Outbound Port Map Low	0242_H	
FGOPML_19	Forwarding Group 19 Outbound Port Map Low	0244_H	
FGOPML_20	Forwarding Group 20 Outbound Port Map Low	0246_H	
FGOPML_21	Forwarding Group 21 Outbound Port Map Low	0248_H	
FGOPML_22	Forwarding Group 22 Outbound Port Map Low	$024A_H$	
FGOPML_23	Forwarding Group 23 Outbound Port Map Low	$024C_H$	
FGOPML_24	Forwarding Group 24 Outbound Port Map Low	$024E_H$	
FGOPML_25	Forwarding Group 25 Outbound Port Map Low	0250_H	
FGOPML_26	Forwarding Group 26 Outbound Port Map Low	0252_H	
FGOPML_27	Forwarding Group 27 Outbound Port Map Low	0254_H	
FGOPML_28	Forwarding Group 28 Outbound Port Map Low	0256_H	
FGOPML_29	Forwarding Group 29 Outbound Port Map Low	0258_H	
FGOPML_30	Forwarding Group 30 Outbound Port Map Low	$025A_H$	
FGOPML_31	Forwarding Group 31 Outbound Port Map Low	$025C_H$	

Forwarding Group 0 Outbound Port Map High

FGOPMH_0 **Offset** **Reset Value**
Forwarding Group 0 Outbound Port Map High **$021F_H$** **$03FF_H$**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res						FG25	FG24	FG23	FG22	FG21	FG20	FG19	FG18	FG17	FG16
						rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
FG25	9	rw	**Forwarding Group Port 25** 0_B , Port 25 is not in the Forwarding Group 1_B , Port 25 is in the Forwarding Group
FG24	8	rw	**Forwarding Group Port 24** 0_B , Port 24 is not in the Forwarding Group 1_B , Port 24 is in the Forwarding Group
FG23	7	rw	**Forwarding Group Port 23** 0_B , Port 23 is not in the Forwarding Group 1_B , Port 23 is in the Forwarding Group
FG22	6	rw	**Forwarding Group Port 22** 0_B , Port 22 is not in the Forwarding Group 1_B , Port 22 is in the Forwarding Group
FG21	5	rw	**Forwarding Group Port 21** 0_B , Port 21 is not in the Forwarding Group 1_B , Port 21 is in the Forwarding Group

Field	Bits	Type	Description
FG20	4	rw	**Forwarding Group Port 20** 0_B , Port 20 is not in the Forwarding Group 1_B , Port 20 is in the Forwarding Group
FG19	3	rw	**Forwarding Group Port 19** 0_B , Port 19 is not in the Forwarding Group 1_B , Port 19 is in the Forwarding Group
FG18	2	rw	**Forwarding Group Port 18** 0_B , Port 18 is not in the Forwarding Group 1_B , Port 18 is in the Forwarding Group
FG17	1	rw	**Forwarding Group Port 17** 0_B , Port 17 is not in the Forwarding Group 1_B , Port 17 is in the Forwarding Group
FG16	0	rw	**Forwarding Group Port 16** 0_B , Port 16 is not in the Forwarding Group 1_B , Port 16 is in the Forwarding Group

All FGOPMH_x registers have the same structure and characteristics, see **FGOPMH_0**. The offset addresses of the other FGOPMH_x registers are listed in **Table 22**.

Table 22 FGOPMH_x Registers

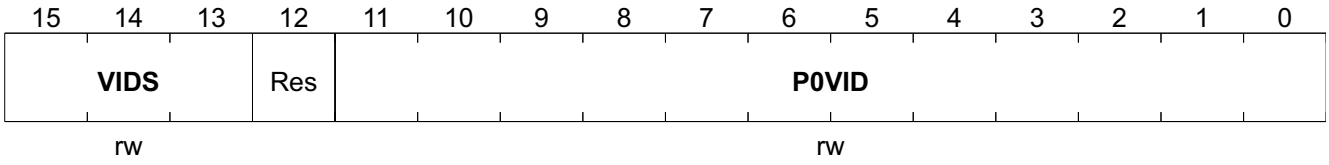
Register Short Name	Register Long Name	Offset Address	Page Number
FGOPMH_1	Forwarding Group 1 Outbound Port Map High	0221_H	
FGOPMH_2	Forwarding Group 2 Outbound Port Map High	0223_H	
FGOPMH_3	Forwarding Group 3 Outbound Port Map High	0225_H	
FGOPMH_4	Forwarding Group 4 Outbound Port Map High	0227_H	
FGOPMH_5	Forwarding Group 5 Outbound Port Map High	0229_H	
FGOPMH_6	Forwarding Group 6 Outbound Port Map High	$022B_H$	
FGOPMH_7	Forwarding Group 7 Outbound Port Map High	$022D_H$	
FGOPMH_8	Forwarding Group 8 Outbound Port Map High	$022F_H$	
FGOPMH_9	Forwarding Group 9 Outbound Port Map High	0231_H	
FGOPMH_10	Forwarding Group 10 Outbound Port Map High	0233_H	
FGOPMH_11	Forwarding Group 11 Outbound Port Map High	0235_H	
FGOPMH_12	Forwarding Group 12 Outbound Port Map High	0237_H	
FGOPMH_13	Forwarding Group 13 Outbound Port Map High	0239_H	
FGOPMH_14	Forwarding Group 14 Outbound Port Map High	$023B_H$	
FGOPMH_15	Forwarding Group 15 Outbound Port Map High	$023D_H$	
FGOPMH_16	Forwarding Group 16 Outbound Port Map High	$023F_H$	
FGOPMH_17	Forwarding Group 17 Outbound Port Map High	0241_H	
FGOPMH_18	Forwarding Group 18 Outbound Port Map High	0243_H	
FGOPMH_19	Forwarding Group 19 Outbound Port Map High	0245_H	
FGOPMH_20	Forwarding Group 20 Outbound Port Map High	0247_H	
FGOPMH_21	Forwarding Group 21 Outbound Port Map High	0249_H	
FGOPMH_22	Forwarding Group 22 Outbound Port Map High	$024B_H$	

Table 22 FGOPMH_x Registers (cont'd)

Register Short Name	Register Long Name	Offset Address	Page Number
FGOPMH_23	Forwarding Group 23 Outbound Port Map High	$024D_H$	
FGOPMH_24	Forwarding Group 24 Outbound Port Map High	$024F_H$	
FGOPMH_25	Forwarding Group 25 Outbound Port Map High	0251_H	
FGOPMH_26	Forwarding Group 26 Outbound Port Map High	0253_H	
FGOPMH_27	Forwarding Group 27 Outbound Port Map High	0255_H	
FGOPMH_28	Forwarding Group 28 Outbound Port Map High	0257_H	
FGOPMH_29	Forwarding Group 29 Outbound Port Map High	0259_H	
FGOPMH_30	Forwarding Group 30 Outbound Port Map High	$025B_H$	
FGOPMH_31	Forwarding Group 31 Outbound Port Map High	$025D_H$	

P0 VID and PVID Shift

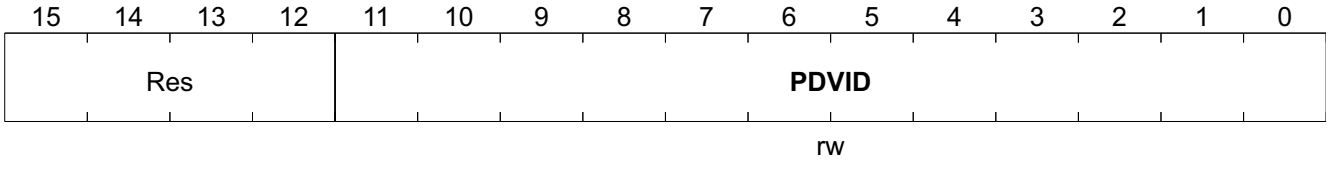
P0VIDS	Offset	Reset Value
P0 VID and PVID Shift	**$025E_H$**	**0001_H**



Field	Bits	Type	Description
VIDS	15:13	rw	**VID Shift** This function maps 4096 VLAN into 32 Forwarding Groups 1. In Tagged Based VLAN, the ADM6926/X will use 5 bits from VID as the Index to map into forwarding groups. 32 forwarding groups are defined in the ADM6926/X. We use F0, F1, … F31 to call each forwarding group. This looking scheme is different from the Port Based VLAN because Port Based VLAN uses port number as the Index to map into the forwarding groups and then F26 ~ F31 will not be used. The VID is defined as follows: • The port's Default VID is used if the frame is not 802.3ac Tagged (No Tag Header in the frame). • The port's Default VID is used if the frame is 802.3ac Tagged (Tag Header in the frame) and the frame's VID is 0000_H or 0001_H and the Enable Replace VLAN ID function is enabled. • The VID in the Tag Header is used if the frame is 802.3 Tagged and the frame's VID is not 0000_H or 0001_H. • The VID in the Tag Header is used if the frame is 802.3 Tagged and the frame's VID is 0000_H or 0001_H and Enable Replace VLAN ID function is not enabled. 2. The relation between VID Shift, VID and the forwarding group is as follows: Bit[15:13] Forwarding Group 000_B , VID[4:0] 001_B , VID[5:1] 010_B , VID[6:2] 011_B , VID[7:3] 100_B , VID[8:4] 101_B , VID[9:5] 110_B , VID[10:6] 111_B , VID[11:7]
P0VID	11:0	rw	**Port 0 VID** The port's Default VID is used if the frame is untagged or if the frame's VID is 0000_H or 0001_H and Enable Replace VLAN ID function (also see **Miscellaneous Configuration** Register) is enabled.

P1 VID Configuration

P1_VID	Offset	Reset Value
P1 VID Configuration	$025F_H$	0001_H



Field	Bits	Type	Description
PDVID	11:0	rw	**The Port's Default VID**

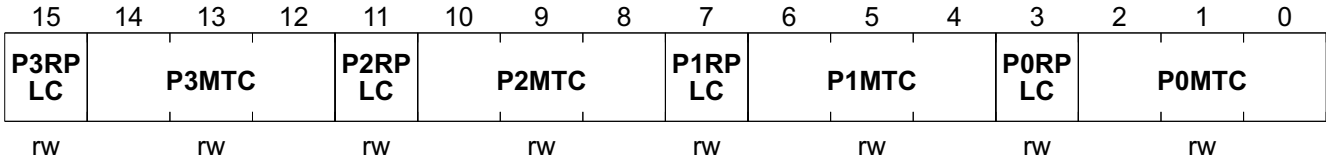
All Px_VID registers have the same structure and characteristics, see **P1_VID**. The offset addresses of the other Px_VID registers are listed in **Table 23**.

Table 23 Px_VID Registers

Register Short Name	Register Long Name	Offset Address	Page Number
P2_VID	P2 VID Configuration	0260_H	
P3_VID	P3 VID Configuration	0261_H	
P4_VID	P4 VID Configuration	0262_H	
P5_VID	P5 VID Configuration	0263_H	
P6_VID	P6 VID Configuration	0264_H	
P7_VID	P7 VID Configuration	0265_H	
P8_VID	P8 VID Configuration	0266_H	
P9_VID	P9 VID Configuration	0267_H	
P10_VID	P10 VID Configuration	0268_H	
P11_VID	P11 VID Configuration	0269_H	
P12_VID	P12 VID Configuration	$026A_H$	
P13_VID	P13 VID Configuration	$026B_H$	
P14_VID	P14 VID Configuration	$026C_H$	
P15_VID	P15 VID Configuration	$026D_H$	
P16_VID	P16 VID Configuration	$026E_H$	
P17_VID	P17 VID Configuration	$026F_H$	
P18_VID	P18 VID Configuration	0270_H	
P19_VID	P19 VID Configuration	0271_H	
P20_VID	P20 VID Configuration	0272_H	
P21_VID	P21 VID Configuration	0273_H	
P22_VID	P22 VID Configuration	0274_H	
P23_VID	P23 VID Configuration	0275_H	
P24_VID	P24 VID Configuration	0276_H	
P25_VID	P25 VID Configuration	0277_H	

P0, P1, P2, P3 Bandwidth Control Register

P0_3_BCR	Offset	Reset Value
P0, P1, P2, P3 Bandwidth Control Register	**0278_H**	**0000_H**



Field	Bits	Type	Description
P3RPLC	15	rw	**Port 3 Receive Packet Length Counted on the Source Port** 0_B , The switch will add length to the P3 counter, default
P3MTC	14:12	rw	**Port 3 Meter Threshold Control** 000_B , 64k, default 001_B , 128k 010_B , 256k 011_B , 512k 100_B , 1M 101_B , 4M 110_B , 10M 111_B , 20M
P2RPLC	11	rw	**Port 2 Receive Packet Length Counted on the Source Port** 0_B , The switch will add length to the P2 counter, default
P2MTC	10:8	rw	**Port 2 Meter Threshold Control** 000_B , 64k, default 001_B , 128k 010_B , 256k 011_B , 512k 100_B , 1M 101_B , 4M 110_B , 10M 111_B , 20M
P1RPLC	7	rw	**Port 1 Receive Packet Length Counted on the Source Port** 0_B , The switch will add length to the P1 counter, default
P1MTC	6:4	rw	**Port 1 Meter Threshold Control** 000_B , 64k, default 001_B , 128k 010_B , 256k 011_B , 512k 100_B , 1M 101_B , 4M 110_B , 10M 111_B , 20M
P0RPLC	3	rw	**Port 0 Receive Packet Length Counted on the Source Port** 0_B , The switch will add length to the P0 counter, default

Field	Bits	Type	Description
P0MTC	2:0	rw	**Port 0 Meter Threshold Control** 000_B , 64k, default 001_B , 128k 010_B , 256k 011_B , 512k 100_B , 1M 101_B , 4M 110_B , 10M 111_B , 20M

P4, P5, P6, P7 Bandwidth Control Register

P4_7_BCR **Offset** **Reset Value**

P4, P5, P6, P7 Bandwidth Control Register **0279_H** **0000_H**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P7RPLC	**P7MTC**			**P6RPLC**	**P6MTC**			**P5RPLC**	**P5MTC**			**P4RPLC**	**P4MTC**		
rw	rw			rw	rw			rw	rw			rw	rw		

Field	Bits	Type	Description
P7RPLC	15	rw	**Port 7 Receive Packet Length Counted on the Source Port** 0_B , The switch will add length to the P7 counter, default
P7MTC	14:12	rw	**Port 7 Meter Threshold Control** 000_B , 64k, default 001_B , 128k 010_B , 256k 011_B , 512k 100_B , 1M 101_B , 4M 110_B , 10M 111_B , 20M
P6RPLC	11	rw	**Port 6 Receive Packet Length Counted on the Source Port** 0_B , The switch will add length to the P6 counter, default
P6MTC	10:8	rw	**Port 6 Meter Threshold Control** 000_B , 64k, default 001_B , 128k 010_B , 256k 011_B , 512k 100_B , 1M 101_B , 4M 110_B , 10M 111_B , 20M
P5RPLC	7	rw	**Port 5 Receive Packet Length Counted on the Source Port** 0_B , The switch will add length to the P5 counter, default

Field	Bits	Type	Description
P5MTC	6:4	rw	**Port 5 Meter Threshold Control** 000_B , 64k, default 001_B , 128k 010_B , 256k 011_B , 512k 100_B , 1M 101_B , 4M 110_B , 10M 111_B , 20M
P4RPLC	3	rw	**Port 4 Receive Packet Length Counted on the Source Port** 0_B , The switch will add length to the P4 counter, default
P4MTC	2:0	rw	**Port 4 Meter Threshold Control** 000_B , 64k, default 001_B , 128k 010_B , 256k 011_B , 512k 100_B , 1M 101_B , 4M 110_B , 10M 111_B , 20M

P8, P9, P10, P11 Bandwidth Control Register

P8_11_BCR — **Offset** — **Reset Value**

P8, P9, P10, P11 Bandwidth Control Register — **$027A_H$** — **0000_H**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P11RPLC	**P11MTC**			**P10RPLC**	**P10MTC**			**P9RPLC**	**P9MTC**			**P8RPLC**	**P8MTC**		
rw	rw			rw	rw			rw	rw			rw	rw		

Field	Bits	Type	Description
P11RPLC	15	rw	**Port 11 Receive Packet Length Counted on the Source Port** 0_B , The switch will add length to the P11 counter, default
P11MTC	14:12	rw	**Port 11 Meter Threshold Control** 000_B , 64k, default 001_B , 128k 010_B , 256k 011_B , 512k 100_B , 1M 101_B , 4M 110_B , 10M 111_B , 20M
P10RPLC	11	rw	**Port 10 Receive Packet Length Counted on the Source Port** 0_B , The switch will add length to the P10 counter, default

Field	Bits	Type	Description
P10MTC	10:8	rw	**Port 10 Meter Threshold Control** 000_B , 64k, default 001_B , 128k 010_B , 256k 011_B , 512k 100_B , 1M 101_B , 4M 110_B , 10M 111_B , 20M
P9RPLC	7	rw	**Port 9 Receive Packet Length Counted on the Source Port** 0_B , The switch will add length to the P9 counter, default
P9MTC	6:4	rw	**Port 9 Meter Threshold Control** 000_B , 64k, default 001_B , 128k 010_B , 256k 011_B , 512k 100_B , 1M 101_B , 4M 110_B , 10M 111_B , 20M
P8RPLC	3	rw	**Port 8 Receive Packet Length Counted on the Source Port** 0_B , The switch will add length to the P8 counter, default
P8MTC	2:0	rw	**Port 8 Meter Threshold Control** 000_B , 64k, default 001_B , 128k 010_B , 256k 011_B , 512k 100_B , 1M 101_B , 4M 110_B , 10M 111_B , 20M

P12, P13, P14, P15 Bandwidth Control Register

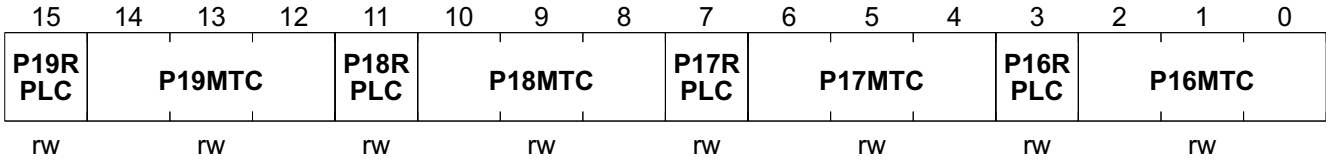
P12_15_BCR	Offset	Reset Value
P12, P13, P14, P15 Bandwidth Control Register	$027B_H$	0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P15R PLC	P15MTC			P14R PLC	P14MTC			P13R PLC	P13MTC			P12R PLC	P12MTC		
rw	rw			rw	rw			rw	rw			rw	rw		

Field	Bits	Type	Description
P15RPLC	15	rw	**Port 15 Receive Packet Length Counted on the Source Port** 0_B , The switch will add length to the P15 counter, default
P15MTC	14:12	rw	**Port 15 Meter Threshold Control** 000_B , 64k, default 001_B , 128k 010_B , 256k 011_B , 512k 100_B , 1M 101_B , 4M 110_B , 10M 111_B , 20M
P14RPLC	11	rw	**Port 14 Receive Packet Length Counted on the Source Port** 0_B , The switch will add length to the P14 counter, default
P14MTC	10:8	rw	**Port 14 Meter Threshold Control** 000_B , 64k, default 001_B , 128k 010_B , 256k 011_B , 512k 100_B , 1M 101_B , 4M 110_B , 10M 111_B , 20M
P13RPLC	7	rw	**Port 13 Receive Packet Length Counted on the Source Port** 0_B , The switch will add length to the P13 counter, default
P13MTC	6:4	rw	**Port 13 Meter Threshold Control** 000_B , 64k, default 001_B , 128k 010_B , 256k 011_B , 512k 100_B , 1M 101_B , 4M 110_B , 10M 111_B , 20M
P12RPLC	3	rw	**Port 12 Receive Packet Length Counted on the Source Port** 0_B , The switch will add length to the P12 counter, default
P12MTC	2:0	rw	**Port 12 Meter Threshold Control** 000_B , 64k, default 001_B , 128k 010_B , 256k 011_B , 512k 100_B , 1M 101_B , 4M 110_B , 10M 111_B , 20M

P16, P17, P18, P19 Bandwidth Control Register

P16_19_BCR	Offset	Reset Value
P16, P17, P18, P19 Bandwidth Control Register	$027C_H$	0000_H



Field	Bits	Type	Description
P19RPLC	15	rw	**Port 19 Receive Packet Length Counted on the Source Port** 0_B , The switch will add length to the P19 counter, default
P19MTC	14:12	rw	**Port 19 Meter Threshold Control** 000_B , 64k, default 001_B , 128k 010_B , 256k 011_B , 512k 100_B , 1M 101_B , 4M 110_B , 10M 111_B , 20M
P18RPLC	11	rw	**Port 18 Receive Packet Length Counted on the Source Port** 0_B , The switch will add length to the P18 counter, default
P18MTC	10:8	rw	**Port 18 Meter Threshold Control** 000_B , 64k, default 001_B , 128k 010_B , 256k 011_B , 512k 100_B , 1M 101_B , 4M 110_B , 10M 111_B , 20M
P17RPLC	7	rw	**Port 17 Receive Packet Length Counted on the Source Port** 0_B , The switch will add length to the P17 counter, default
P17MTC	6:4	rw	**Port 17 Meter Threshold Control** 000_B , 64k, default 001_B , 128k 010_B , 256k 011_B , 512k 100_B , 1M 101_B , 4M 110_B , 10M 111_B , 20M
P16RPLC	3	rw	**Port 16 Receive Packet Length Counted on the Source Port** 0_B , The switch will add length to the P16 counter, default

Field	Bits	Type	Description
P16MTC	2:0	rw	**Port 16 Meter Threshold Control** 000_B , 64k, default 001_B , 128k 010_B , 256k 011_B , 512k 100_B , 1M 101_B , 4M 110_B , 10M 111_B , 20M

P20, P21, P22, P23 Bandwidth Control Register

P20_23_BCR	Offset	Reset Value
P20, P21, P22, P23 Bandwidth Control Register	$027D_H$	0000_H

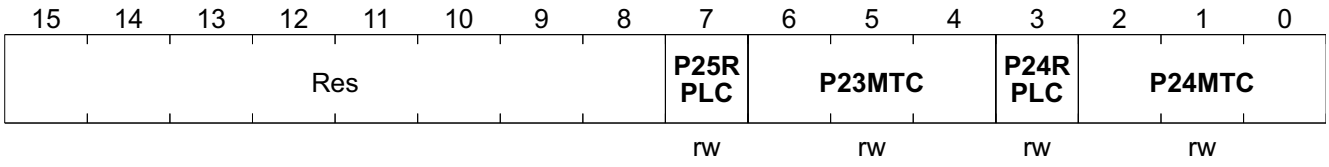
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P23RPLC	P23MTC			P22RPLC	P22MTC			P21RPLC	P21MTC			P20RPLC	P20MTC		
rw	rw			rw	rw			rw	rw			rw	rw		

Field	Bits	Type	Description
P23RPLC	15	rw	**Port 23 Receive Packet Length Counted on the Source Port** 0_B , The switch will add length to the P23 counter, default
P23MTC	14:12	rw	**Port 23 Meter Threshold Control** 000_B , 64k, default 001_B , 128k 010_B , 256k 011_B , 512k 100_B , 1M 101_B , 4M 110_B , 10M 111_B , 20M
P22RPLC	11	rw	**Port 22 Receive Packet Length Counted on the Source Port** 0_B , The switch will add length to the P22 counter, default
P22MTC	10:8	rw	**Port 22 Meter Threshold Control** 000_B , 64k, default 001_B , 128k 010_B , 256k 011_B , 512k 100_B , 1M 101_B , 4M 110_B , 10M 111_B , 20M

Field	Bits	Type	Description
P21RPLC	7	rw	**Port 21 Receive Packet Length Counted on the Source Port** 0_B , The switch will add length to the P21 counter, default
P21MTC	6:4	rw	**Port 21 Meter Threshold Control** 000_B , 64k, default 001_B , 128k 010_B , 256k 011_B , 512k 100_B , 1M 101_B , 4M 110_B , 10M 111_B , 20M
P20RPLC	3	rw	**Port 20 Receive Packet Length Counted on the Source Port** 0_B , The switch will add length to the P20 counter, default
P20MTC	2:0	rw	**Port 20 Meter Threshold Control** 000_B , 64k, default 001_B , 128k 010_B , 256k 011_B , 512k 100_B , 1M 101_B , 4M 110_B , 10M 111_B , 20M

P24, P25 Bandwidth Control Register

P24_25_BCR	**Offset**	**Reset Value**
P24, P25 Bandwidth Control Register	**$027E_H$**	**0000_H**



Field	Bits	Type	Description
P25RPLC	7	rw	**Port 25 Receive Packet Length Counted on the Source Port** 0_B , The switch will add length to the P25 counter, default
P23MTC	6:4	rw	**Port 25 Meter Threshold Control** 000_B , 64k, default 001_B , 128k 010_B , 256k 011_B , 512k 100_B , 1M 101_B , 4M 110_B , 10M 111_B , 20M

Field	Bits	Type	Description
P24RPLC	3	rw	**Port 24 Receive Packet Length Counted on the Source Port** 0_B , The switch will add length to the P24 counter, default
P24MTC	2:0	rw	**Port 24 Meter Threshold Control** 000_B , 64k, default 001_B , 128k 010_B , 256k 011_B , 512k 100_B , 1M 101_B , 4M 110_B , 10M 111_B , 20M

Bandwidth Control Enable Register Low

BCERL	Offset	Reset Value
Bandwidth Control Enable Register Low	**$027F_H$**	**0000_H**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BCEP 15	**BCEP 14**	**BCEP 13**	**BCEP 12**	**BCEP 11**	**BCEP 10**	**BCEP 9**	**BCEP 8**	**BCEP 7**	**BCEP 6**	**BCEP 5**	**BCEP 4**	**BCEP 3**	**BCEP 2**	**BCEP 1**	**BCEP 0**
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
BCEP15	15	rw	**Bandwidth Control Enable for Port 15**
BCEP14	14	rw	**Bandwidth Control Enable for Port 14**
BCEP13	13	rw	**Bandwidth Control Enable for Port 13**
BCEP12	12	rw	**Bandwidth Control Enable for Port 12**
BCEP11	11	rw	**Bandwidth Control Enable for Port 11**
BCEP10	10	rw	**Bandwidth Control Enable for Port 10**
BCEP9	9	rw	**Bandwidth Control Enable for Port 9**
BCEP8	8	rw	**Bandwidth Control Enable for Port 8**
BCEP7	7	rw	**Bandwidth Control Enable for Port 7**
BCEP6	6	rw	**Bandwidth Control Enable for Port 6**
BCEP5	5	rw	**Bandwidth Control Enable for Port 5**
BCEP4	4	rw	**Bandwidth Control Enable for Port 4**
BCEP3	3	rw	**Bandwidth Control Enable for Port 3**
BCEP2	2	rw	**Bandwidth Control Enable for Port 2**
BCEP1	1	rw	**Bandwidth Control Enable for Port 1**
BCEP0	0	rw	**Bandwidth Control Enable for Port 0** 0_B , Port 0 disables the bandwidth control. 1_B , Port 0 enables the bandwidth control.

Bandwidth Control Enable Register High

BCERH	Offset	Reset Value
Bandwidth Control Enable Register High	**0280_H**	**0000_H**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res						BCEP 25	BCEP 24	BCEP 23	BCEP 22	BCEP 21	BCEP 20	BCEP 19	BCEP 18	BCEP 17	BCEP 16
						rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
BCEP25	9	rw	**Bandwidth Control Enable for Port 25**
BCEP24	8	rw	**Bandwidth Control Enable for Port 24**
BCEP23	7	rw	**Bandwidth Control Enable for Port 23**
BCEP22	6	rw	**Bandwidth Control Enable for Port 22**
BCEP21	5	rw	**Bandwidth Control Enable for Port 21**
BCEP20	4	rw	**Bandwidth Control Enable for Port 20**
BCEP19	3	rw	**Bandwidth Control Enable for Port 19**
BCEP18	2	rw	**Bandwidth Control Enable for Port 18**
BCEP17	1	rw	**Bandwidth Control Enable for Port 17**
BCEP16	0	rw	**Bandwidth Control Enable for Port 16**

Reserved Register 1

RES1	Offset	Reset Value
Reserved Register 1	**0281_H**	**0000_H**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res															
ro															

Field	Bits	Type	Description
Res	15:0	ro	**Reserved** For the future use and don't modify the values. Default: See **Chapter 3.2**

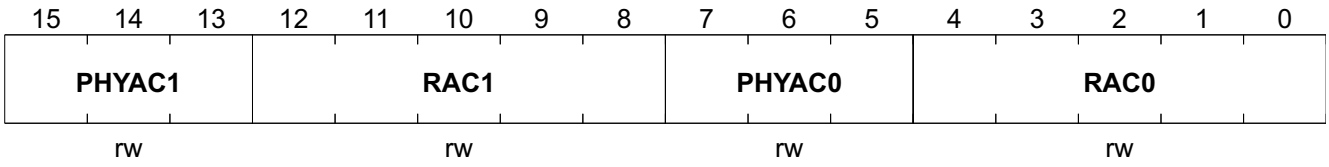
All RESx registers have the same structure and characteristics, see **RES1**. The offset addresses of the other RESx registers are listed in **Table 24**.

Table 24 RESx Registers

Register Short Name	Register Long Name	Offset Address	Page Number
RES2	Reserved Register 2	0282_H	
RES3	Reserved Register 3	0283_H	
RES4	Reserved Register 4	0284_H	
RES5	Reserved Register 5	0285_H	
RES6	Reserved Register 6	0286_H	
RES7	Reserved Register 7	0287_H	
RES8	Reserved Register 8	0288_H	
RES9	Reserved Register 9	0289_H	
RES10	Reserved Register 10	$028A_H$	

Customized PHY Control Group 0

CPHYCG0	Offset	Reset Value
Customized PHY Control Group 0	$028B_H$	0000_H



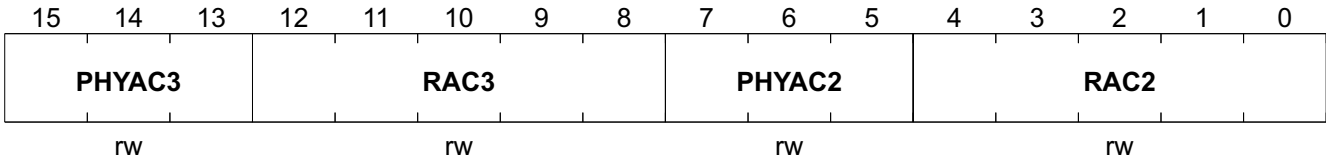
Field	Bits	Type	Description
PHYAC1	15:13	rw	**PHY Address of the Command 1** If Bit[2:0] in PHY Customized Enable Register = 3'b010 or 3'b011. 000_B , The switch will write command 1 into Port 0 (PHY Address = 32'h8). 001_B , The switch will write command 1 into Port 1 (PHY Address = 32'h9). 010_B , The switch will write command 1 into Port 2 (PHY Address = 32'ha). 011_B , The switch will write command 1 into Port 3 (PHY Address = 32'hb). 100_B , The switch will write command 1 into Port 4 (PHY Address = 32'hc). 101_B , The switch will write command 1 into Port 5 (PHY Address = 32'hd). 110_B , The switch will write command 1 into Port 6 (PHY Address = 32'he). 111_B , The switch will write command 1 into Port 7 (PHY Address = 32'hf).
RAC1	12:8	rw	**Register Address of the Command 1**

Field	Bits	Type	Description
PHYAC0	7:5	rw	**PHY Address of the Command 0** If Bit[2:0] in PHY Customized Enable Register = 3'b001 or 3'b011. 000_B , The switch will write command 0 into Port 0 (PHY Address = 32'h8). 001_B , The switch will write command 0 into Port 1 (PHY Address = 32'h9). 010_B , The switch will write command 0 into Port 2 (PHY Address = 32'ha). 011_B , The switch will write command 0 into Port 3 (PHY Address = 32'hb). 100_B , The switch will write command 0 into Port 4 (PHY Address = 32'hc). 101_B , The switch will write command 0 into Port 5 (PHY Address = 32'hd). 110_B , The switch will write command 0 into Port 6 (PHY Address = 32'he). 111_B , The switch will write command 0 into Port 7 (PHY Address = 32'hf).
RAC0	4:0	rw	**Register Address of the Command 0**

Note: The ADM6926/X supports eight additional commands for the customer to configure the PHY attached. Four groups are defined and each group shares two commands. Group 0 contains P0, P1, P2, P3, P4, P5, P6 and P7. Group 1 contains P8, P9, P10, P11, P12, P13, P14 and P15. Group 2 contains P16, P17, P18, P19, P20, P21, P22 and P23. Group 3 contains P24 and P25. 3 bits enable register is associated with each group. Each command is associated with a PHY address, a register address, and data for writing.

Customized PHY Control Group 1

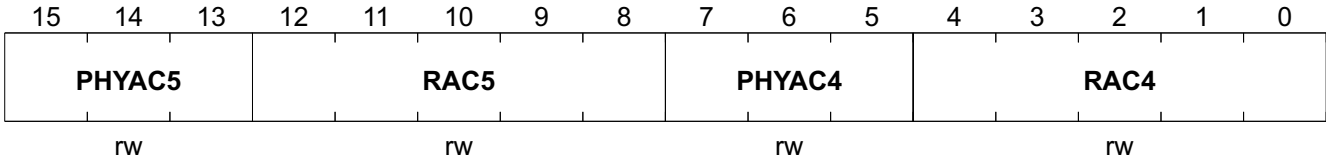
CPHYCG1	Offset	Reset Value
Customized PHY Control Group 1	$028C_H$	0000_H



Field	Bits	Type	Description
PHYAC3	15:13	rw	**PHY Address of the Command 3** Bit[5:3] in PHY Customized Enable Register = 3'b010 or 3'b011. 000_B , The switch will write command 3 into Port 8 (PHY Address = 32'h10). 001_B , The switch will write command 3 into Port 9 (PHY Address = 32'h11). 010_B , The switch will write command 3 into Port 10 (PHY Address = 32'h12). 011_B , The switch will write command 3 into Port 11 (PHY Address = 32'h13). 100_B , The switch will write command 3 into Port 12 (PHY Address = 32'h14). 101_B , The switch will write command 3 into Port 13 (PHY Address = 32'h15). 110_B , The switch will write command 3 into Port 14 (PHY Address = 32'h16). 111_B , The switch will write command 3 into Port 15 (PHY Address = 32'h17).
RAC3	12:8	rw	**Register Address of the Command 3**
PHYAC2	7:5	rw	**PHY Address of the Command 2** Bit[5:3] in PHY Customized Enable Register = 3'b001 or 3'b011. 000_B , The switch will write command 2 into Port 8 (PHY Address = 32'h10). 001_B , The switch will write command 2 into Port 9 (PHY Address = 32'h11). 010_B , The switch will write command 2 into Port 10 (PHY Address = 32'h12). 011_B , The switch will write command 2 into Port 11 (PHY Address = 32'h13). 100_B , The switch will write command 2 into Port 12 (PHY Address = 32'h14). 101_B , The switch will write command 2 into Port 13 (PHY Address = 32'h15). 110_B , The switch will write command 2 into Port 14 (PHY Address = 32'h16). 111_B , The switch will write command 2 into Port 15 (PHY Address = 32'h17).
RAC2	4:0	rw	**Register Address of the Command 2**

Customized PHY Control Group 2

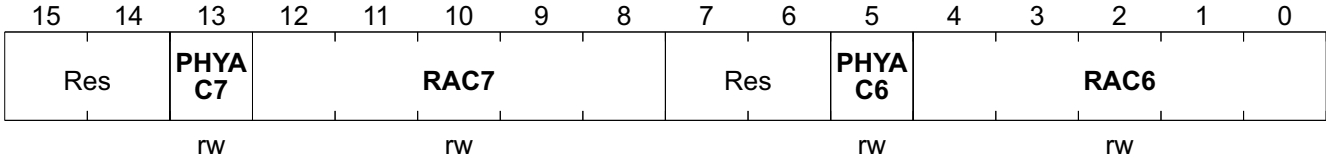
CPHYCG2	Offset	Reset Value
Customized PHY Control Group 2	$028D_H$	0000_H



Field	Bits	Type	Description
PHYAC5	15:13	rw	**PHY Address of the Command 5** Bit[8:6] in PHY Customized Enable Register = 3'b010 or 3'b011. 000_B , The switch will write command 5 into Port 16 (PHY Address = 32'h18). 001_B , The switch will write command 5 into Port 17 (PHY Address = 32'h19). 010_B , The switch will write command 5 into Port 18 (PHY Address = 32'h1a). 011_B , The switch will write command 5 into Port 19 (PHY Address = 32'h1b). 100_B , The switch will write command 5 into Port 20 (PHY Address = 32'h1c). 101_B , The switch will write command 5 into Port 21 (PHY Address = 32'h1d). 110_B , The switch will write command 5 into Port 22 (PHY Address = 32'h1e). 111_B , The switch will write command 5 into Port 23 (PHY Address = 32'h1f).
RAC5	12:8	rw	**Register Address of the Command 5**
PHYAC4	7:5	rw	**PHY Address of the Command 4** Bit[8:6] in PHY Customized Enable Register = 3'b001 or 3'b011. 000_B , The switch will write command 4 into Port 16 (PHY Address = 32'h18). 001_B , The switch will write command 4 into Port 17 (PHY Address = 32'h19). 010_B , The switch will write command 4 into Port 18 (PHY Address = 32'h1a). 011_B , The switch will write command 4 into Port 19 (PHY Address = 32'h1b). 100_B , The switch will write command 4 into Port 20 (PHY Address = 32'h1c). 101_B , The switch will write command 4 into Port 21 (PHY Address = 32'h1d). 110_B , The switch will write command 4 into Port 22 (PHY Address = 32'h1e). 111_B , The switch will write command 4 into Port 23 (PHY Address = 32'h1f).
RAC4	4:0	rw	**Register Address of the Command 4**

Customized PHY Control Group 3

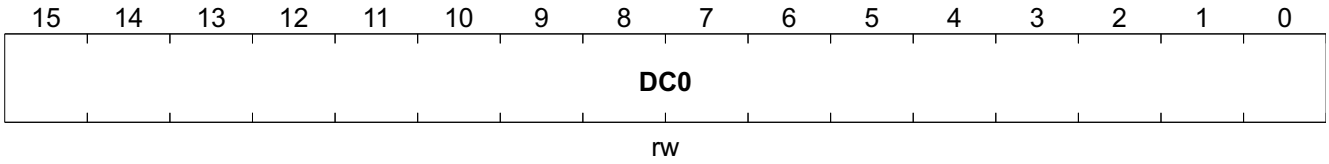
CPHYCG3 | **Offset** | **Reset Value**
Customized PHY Control Group 3 | **$028E_H$** | **0000_H**



Field	Bits	Type	Description
PHYAC7	13	rw	**PHY Address of the Command 7** Bit[11:9] in PHY Customized Enable Register = 3'b010 or 3'b011. 0_B , The switch will write command 7 into Port 24 (PHY Address = 32'h6). 1_B , The switch will write command 7 into Port 25 (PHY Address = 32'h7).
RAC7	12:8	rw	**Register Address of the Command 7**
PHYAC6	5	rw	**PHY Address of the Command 6** Bit[11:9] in PHY Customized Enable Register = 3'b001 or 3'b011. 0_B , The switch will write command 6 into Port 24 (PHY Address = 32'h6). 1_B , The switch will write command 6 into Port 25 (PHY Address = 32'h7).
RAC6	4:0	rw	**Register Address of the Command 6**

Group 0 PHY Customized DATA 0

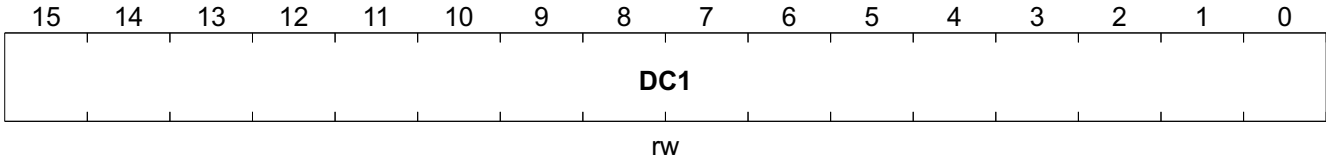
G0PHYCD0 | **Offset** | **Reset Value**
Group 0 PHY Customized DATA 0 | **$028F_H$** | **0000_H**



Field	Bits	Type	Description
DC0	15:0	rw	**Data for Command 0**

Group 0 PHY Customized DATA 1

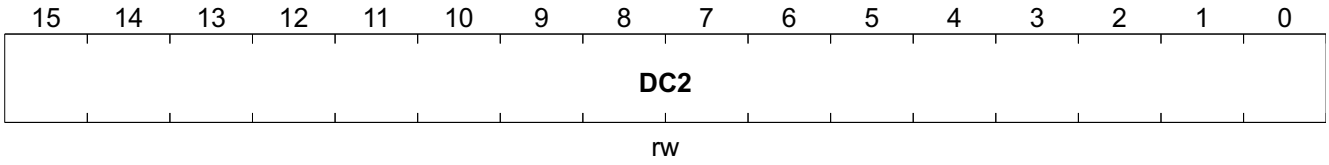
G0PHYCD1 | **Offset** | **Reset Value**
Group 0 PHY Customized DATA 1 | **0290_H** | **0000_H**



Field	Bits	Type	Description
DC1	15:0	rw	**Data for Command 1**

Group 1 PHY Customized DATA 0

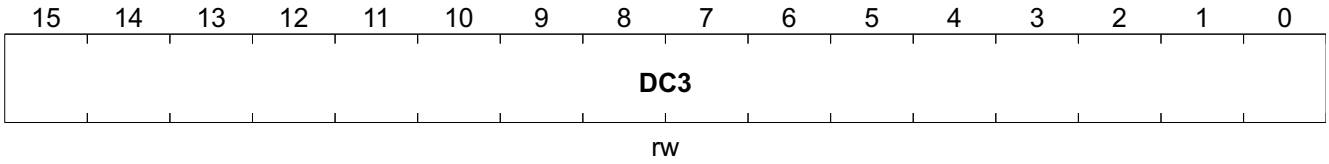
G1PHYCD0 **Offset** **Reset Value**
Group 1 PHY Customized DATA 0 **0291_H** **0000_H**



Field	Bits	Type	Description
DC2	15:0	rw	**Data for Command 2**

Group 1 PHY Customized DATA 1

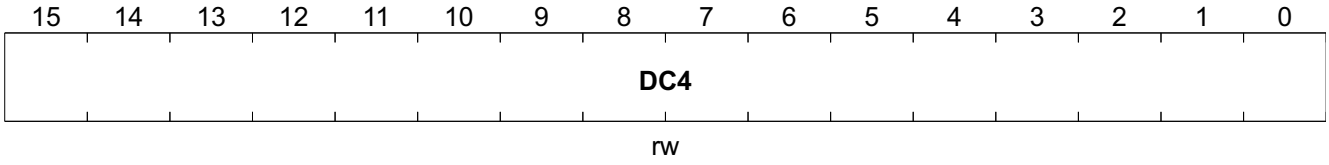
G1PHYCD1 **Offset** **Reset Value**
Group 1 PHY Customized DATA 1 **0292_H** **0000_H**



Field	Bits	Type	Description
DC3	15:0	rw	**Data for Command 3**

Group 2 PHY Customized DATA 0

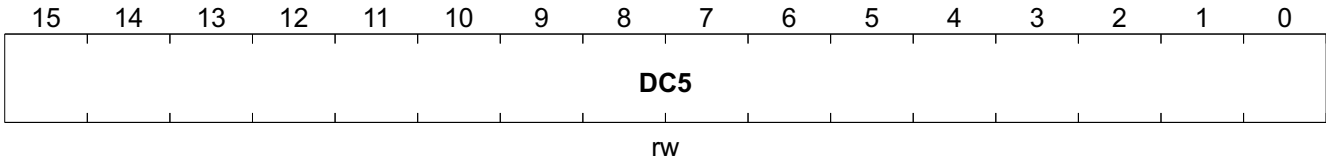
G2PHYCD0 **Offset** **Reset Value**
Group 2 PHY Customized DATA 0 **0293_H** **0000_H**



Field	Bits	Type	Description
DC4	15:0	rw	**Data for Command 4**

Group 2 PHY Customized DATA 1

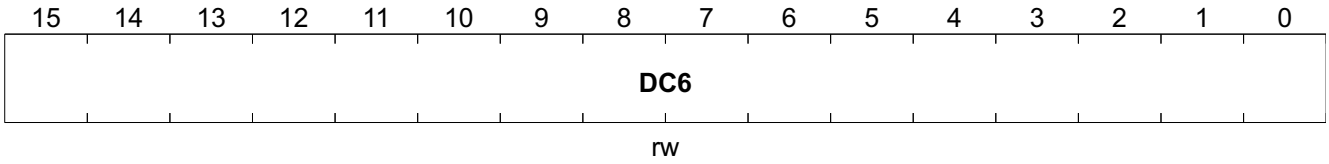
G2PHYCD1 **Offset** **Reset Value**
Group 2 PHY Customized DATA 1 **0294_H** **0000_H**



Field	Bits	Type	Description
DC5	15:0	rw	**Data for Command 5**

Group 3 PHY Customized DATA 0

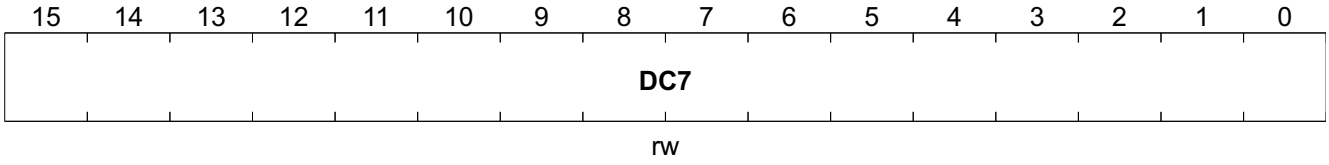
G3PHYCD0 **Offset** **Reset Value**
Group 3 PHY Customized DATA 0 **0295_H** **0000_H**



Field	Bits	Type	Description
DC6	15:0	rw	**Data for Command 6**

Group 3 PHY Customized DATA 1

G3PHYCD1 **Offset** **Reset Value**
Group 3 PHY Customized DATA 1 **0296_H** **0000_H**

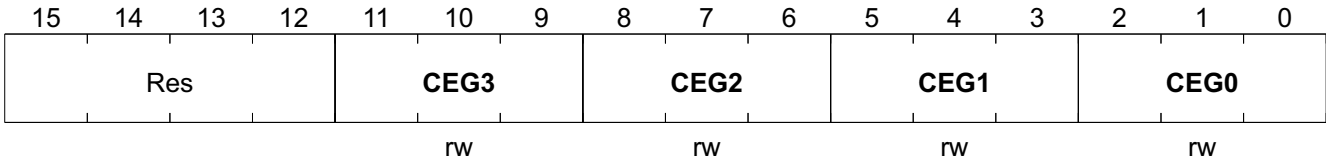


Field	Bits	Type	Description
DC7	15:0	rw	**Data for Command 7**

PHY Customized Enable Register

PHYCE **Offset** **Reset Value**

PHY Customized Enable Register **0297_H** **0000_H**



Field	Bits	Type	Description
CEG3	11:9	rw	**PHY Customized Enable For Group 3** 000_B , Disable writing additional commands into any PHYs in Group 3. 001_B , Write command 6 into related port specified by the Customized PHY Control Group 3. 010_B , Write command 7 into related port specified by the Customized PHY Control Group 3. 100_B , Disable writing additional commands into any PHYs in Group 3. 101_B , Write command 6 into all PHYs in Group 3. 110_B , Write command 7 into all PHYs in Group 3. 111_B , Write command 6 and command 7 into all PHYs in Group 3.
CEG2	8:6	rw	**PHY Customized Enable For Group 2** 000_B , Disable writing additional commands into any PHYs in Group 2. 001_B , Write command 4 into related port specified by the Customized PHY Control Group 2. 010_B , Write command 5 into related port specified by the Customized PHY Control Group 2. 100_B , Disable writing additional commands into any PHYs in Group 2. 101_B , Write command 4 into all PHYs in Group 2. 110_B , Write command 5 into all PHYs in Group 2. 111_B , Write command 5 and command 5 into all PHYs in Group 2.

Field	Bits	Type	Description
CEG1	5:3	rw	**PHY Customized Enable For Group 1** 000_B , Disable writing additional commands into any PHYs in Group 1. 001_B , Write command 2 into related port specified by the Customized PHY Control Group 1. 010_B , Write command 3 into related port specified by the Customized PHY Control Group 1. 100_B , Disable writing additional commands into any PHYs in Group 1. 101_B , Write command 2 into all PHYs in Group 1. 110_B , Write command 3 into all PHYs in Group 1. 111_B , Write command 2 and command 3 into all PHYs in Group 1.
CEG0	2:0	rw	**PHY Customized Enable For Group 0** 000_B , Disable writing additional commands into any PHYs in Group 0. 001_B , Write command 0 into related port specified by the Customized PHY Control Group 0. 010_B , Write command 1 into related port specified by the Customized PHY Control Group 0. 100_B , Disable writing additional commands into any PHYs in Group 0. 101_B , Write command 0 into all PHYs in Group 0. 110_B , Write command 1 into all PHYs in Group 0. 111_B , Write command 0 and command 1 into all PHYs in Group 0.

PPPOE Control Register 0

PPPOEC0	Offset	Reset Value
PPPOE Control Register 0	0298_H	0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EP15TP	EP14TP	EP13TP	EP12TP	EP11TP	EP10TP	EP9TP	EP8TP	EP7TP	EP6TP	EP5TP	EP4TP	EP3TP	EP2TP	EP1TP	EP0TP
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
EP15TP	15	rw	**Enable Port 15 to Transmit PPPoE Packet Only**
EP14TP	14	rw	**Enable Port 14 to Transmit PPPoE Packet Only**
EP13TP	13	rw	**Enable Port 13 to Transmit PPPoE Packet Only**
EP12TP	12	rw	**Enable Port 12 to Transmit PPPoE Packet Only**
EP11TP	11	rw	**Enable Port 11 to Transmit PPPoE Packet Only**
EP10TP	10	rw	**Enable Port 10 to Transmit PPPoE Packet Only**
EP9TP	9	rw	**Enable Port 9 to Transmit PPPoE Packet Only**
EP8TP	8	rw	**Enable Port 8 to Transmit PPPoE Packet Only**
EP7TP	7	rw	**Enable Port 7 to Transmit PPPoE Packet Only**
EP6TP	6	rw	**Enable Port 6 to Transmit PPPoE Packet Only**
EP5TP	5	rw	**Enable Port 5 to Transmit PPPoE Packet Only**

Field	Bits	Type	Description
EP4TP	4	rw	**Enable Port 4 to Transmit PPPoE Packet Only**
EP3TP	3	rw	**Enable Port 3 to Transmit PPPoE Packet Only**
EP2TP	2	rw	**Enable Port 2 to Transmit PPPoE Packet Only**
EP1TP	1	rw	**Enable Port 1 to Transmit PPPoE Packet Only**
EP0TP	0	rw	**Enable Port 0 to Transmit PPPoE Packet Only** The ADM6926/X will recognize packets with length-type = 16'h8863 or 16'h8864 as the PPPOE packets. 0_B , The port 0 is not configured to transmit PPPOE packets only. 1_B , The port 0 is configured to transmit PPPOE packets only.

PPPOE Control Register 1

PPPOEC1	Offset	Reset Value
PPPOE Control Register 1	**0299_H**	**0000_H**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res					**EMPC**	**EP25 TP**	**EP24 TP**	**EP23 TP**	**EP22 TP**	**EP21 TP**	**EP20 TP**	**EP19 TP**	**EP18 TP**	**EP17 TP**	**EP16 TP**
					rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
EMPC	10	rw	**Enable Management Packet Cross PPPOE PORT Function** 0_B , Management packets could not be transmitted by the PPPOE port. 1_B , Management packets could be transmitted by any port even if it is configured to PPPOE port.
EP25TP	9	rw	**Enable Port 25 to Transmit PPPoE Packet Only**
EP24TP	8	rw	**Enable Port 24 to Transmit PPPoE Packet Only**
EP23TP	7	rw	**Enable Port 23 to Transmit PPPoE Packet Only**
EP22TP	6	rw	**Enable Port 22 to Transmit PPPoE Packet Only**
EP21TP	5	rw	**Enable Port 21 to Transmit PPPoE Packet Only**
EP20TP	4	rw	**Enable Port 20 to Transmit PPPoE Packet Only**
EP19TP	3	rw	**Enable Port 19 to Transmit PPPoE Packet Only**
EP18TP	2	rw	**Enable Port 18 to Transmit PPPoE Packet Only**
EP17TP	1	rw	**Enable Port 17 to Transmit PPPoE Packet Only**
EP16TP	0	rw	**Enable Port 16 to Transmit PPPoE Packet Only**

PHY Control Register 0

PHYCR0	Offset	Reset Value
PHY Control Register 0	**$029A_H$**	**0000_H**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY15	**PHY14**	**PHY13**	**PHY12**	**PHY11**	**PHY10**	**PHY9**	**PHY8**	**PHY7**	**PHY6**	**PHY5**	**PHY4**	**PHY3**	**PHY2**	**PHY1**	**PHY0**
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
PHY15	15	rw	**PHY Port 15** 0_B , PHY acts as the slave. 1_B , PHY attached to port 15 acts as the master.
PHY14	14	rw	**PHY Port 14** 0_B , PHY acts as the slave. 1_B , PHY attached to port 14 acts as the master.
PHY13	13	rw	**PHY Port 13** 0_B , PHY acts as the slave. 1_B , PHY attached to port 13 acts as the master.
PHY12	12	rw	**PHY Port 12** 0_B , PHY acts as the slave. 1_B , PHY attached to port 12 acts as the master.
PHY11	11	rw	**PHY Port 11** 0_B , PHY acts as the slave. 1_B , PHY attached to port 11 acts as the master.
PHY10	10	rw	**PHY Port 10** 0_B , PHY acts as the slave. 1_B , PHY attached to port 10 acts as the master.
PHY9	9	rw	**PHY Port 9** 0_B , PHY acts as the slave. 1_B , PHY attached to port 9 acts as the master.
PHY8	8	rw	**PHY Port 8** 0_B , PHY acts as the slave. 1_B , PHY attached to port 8 acts as the master.
PHY7	7	rw	**PHY Port 7** 0_B , PHY acts as the slave. 1_B , PHY attached to port 7 acts as the master.
PHY6	6	rw	**PHY Port 6** 0_B , PHY acts as the slave. 1_B , PHY attached to port 6 acts as the master.
PHY5	5	rw	**PHY Port 5** 0_B , PHY acts as the slave. 1_B , PHY attached to port 5 acts as the master.
PHY4	4	rw	**PHY Port 4** 0_B , PHY acts as the slave. 1_B , PHY attached to port 4 acts as the master.
PHY3	3	rw	**PHY Port 3** 0_B , PHY acts as the slave. 1_B , PHY attached to port 3 acts as the master.

Field	Bits	Type	Description
PHY2	2	rw	**PHY Port 2** 0_B , PHY acts as the slave. 1_B , PHY attached to port 2 acts as the master.
PHY1	1	rw	**PHY Port 1** 0_B , PHY acts as the slave. 1_B , PHY attached to port 1 acts as the master.
PHY0	0	rw	**PHY Port 0** 0_B , PHY acts as the slave. The switch will use the setting in the eeprom register to manage PHY attached. 1_B , PHY attached to port 0 acts as the master. That is the switch will not configure the PHY attached and it will only poll the PHY to know the state that PHY operates.

PHY Control Register 1

PHYCR1 **Offset** **Reset Value**

PHY Control Register 1 **$029B_H$** **0000_H**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res						**PHY25**	**PHY24**	**PHY23**	**PHY22**	**PHY21**	**PHY20**	**PHY19**	**PHY18**	**PHY17**	**PHY16**
						rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
PHY25	9	rw	**PHY Port 25** 0_B , PHY acts as the slave. 1_B , PHY attached to port 25 acts as the master.
PHY24	8	rw	**PHY Port 24** 0_B , PHY acts as the slave. 1_B , PHY attached to port 24 acts as the master.
PHY23	7	rw	**PHY Port 23** 0_B , PHY acts as the slave. 1_B , PHY attached to port 23 acts as the master.
PHY22	6	rw	**PHY Port 22** 0_B , PHY acts as the slave. 1_B , PHY attached to port 22 acts as the master.
PHY21	5	rw	**PHY Port 21** 0_B , PHY acts as the slave. 1_B , PHY attached to port 21 acts as the master.
PHY20	4	rw	**PHY Port 20** 0_B , PHY acts as the slave. 1_B , PHY attached to port 20 acts as the master.

Field	Bits	Type	Description
PHY19	3	rw	**PHY Port 19** 0_B , PHY acts as the slave. 1_B , PHY attached to port 19 acts as the master.
PHY18	2	rw	**PHY Port 18** 0_B , PHY acts as the slave. 1_B , PHY attached to port 18 acts as the master.
PHY17	1	rw	**PHY Port 17** 0_B , PHY acts as the slave. 1_B , PHY attached to port 17 acts as the master.
PHY16	0	rw	**PHY Port 16** 0_B , PHY acts as the slave. 1_B , PHY attached to port 16 acts as the master.

Disable MDIO Active Register 0

DMDIOAR0	Offset	Reset Value
Disable MDIO Active Register 0	$029C_H$	0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P15BMFE	P14BMFE	P13BMFE	P12BMFE	P11BMFE	P10BMFE	P9BMFE	P8BMFE	P7BMFE	P6BMFE	P5BMFE	P4BMFE	P3BMFE	P2BMFE	P1BMFE	P0BMFE
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
P15BMFE	15	rw	**Port 15 Bypass MDIO Function Enable**
P14BMFE	14	rw	**Port 14 Bypass MDIO Function Enable**
P13BMFE	13	rw	**Port 13 Bypass MDIO Function Enable**
P12BMFE	12	rw	**Port 12 Bypass MDIO Function Enable**
P11BMFE	11	rw	**Port 11 Bypass MDIO Function Enable**
P10BMFE	10	rw	**Port 10 Bypass MDIO Function Enable**
P9BMFE	9	rw	**Port 9 Bypass MDIO Function Enable**
P8BMFE	8	rw	**Port 8 Bypass MDIO Function Enable**
P7BMFE	7	rw	**Port 7 Bypass MDIO Function Enable**
P6BMFE	6	rw	**Port 6 Bypass MDIO Function Enable**
P5BMFE	5	rw	**Port 5 Bypass MDIO Function Enable**
P4BMFE	4	rw	**Port 4 Bypass MDIO Function Enable**
P3BMFE	3	rw	**Port 3 Bypass MDIO Function Enable**
P2BMFE	2	rw	**Port 2 Bypass MDIO Function Enable**
P1BMFE	1	rw	**Port 1 Bypass MDIO Function Enable**

Field	Bits	Type	Description
P0BMFE	0	rw	**Port 0 Bypass MDIO Function Enable** 0_B , Bypass MDIO Disable. The status is dominated by the MDC/MDIO function except the linkup status, which may be disabled, by the port disable function or the spanning protocol. 1_B , Bypass MDIO Enable. The effect by the function is as follows: Link Status: Port 0 is forced to link up unless the port is disabled or the spanning tree is in disabled state. Speed Status: Port 0 is configured to Bit [6] in the Port Configuration Register. Duplex Status: Port 0 is configured to Bit [7] in the Port Configuration Register. Pause Status: Port 0 is configured to Bit [4] in the Port Configuration Register. Back Pressure Status: Port 0 is configured to Bit[15] in the Port Configuration Register.

Disable MDIO Active Register 1

DMDIOAR1	Offset	Reset Value
Disable MDIO Active Register 1	**$029D_H$**	**0000_H**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res						P25BMFE	P24BMFE	P23BMFE	P22BMFE	P21BMFE	P20BMFE	P19BMFE	P18BMFE	P17BMFE	P16BMFE
						rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
P25BMFE	9	rw	**Port 25 Bypass MDIO Function Enable**
P24BMFE	8	rw	**Port 24 Bypass MDIO Function Enable**
P23BMFE	7	rw	**Port 23 Bypass MDIO Function Enable**
P22BMFE	6	rw	**Port 22 Bypass MDIO Function Enable**
P21BMFE	5	rw	**Port 21 Bypass MDIO Function Enable**
P20BMFE	4	rw	**Port 20 Bypass MDIO Function Enable**
P19BMFE	3	rw	**Port 19 Bypass MDIO Function Enable**
P18BMFE	2	rw	**Port 18 Bypass MDIO Function Enable**
P17BMFE	1	rw	**Port 17 Bypass MDIO Function Enable**
P16BMFE	0	rw	**Port 16 Bypass MDIO Function Enable**

Port Disable Register 0

PDR0	Offset	Reset Value
Port Disable Register 0	**$029E_H$**	**0000_H**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P15DRT	P14DRT	P13DRT	P12DRT	P11DRT	P10DRT	P9DRT	P8DRT	P7DRT	P6DRT	P5DRT	P4DRT	P3DRT	P2DRT	P1DRT	P0DRT
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
P15DRT	15	rw	**Port 15 Disable Receive and Transmit**
P14DRT	14	rw	**Port 14 Disable Receive and Transmit**
P13DRT	13	rw	**Port 13 Disable Receive and Transmit**
P12DRT	12	rw	**Port 12 Disable Receive and Transmit**
P11DRT	11	rw	**Port 11 Disable Receive and Transmit**
P10DRT	10	rw	**Port 10 Disable Receive and Transmit**
P9DRT	9	rw	**Port 9 Disable Receive and Transmit**
P8DRT	8	rw	**Port 8 Disable Receive and Transmit**
P7DRT	7	rw	**Port 7 Disable Receive and Transmit**
P6DRT	6	rw	**Port 6 Disable Receive and Transmit**
P5DRT	5	rw	**Port 5 Disable Receive and Transmit**
P4DRT	4	rw	**Port 4 Disable Receive and Transmit**
P3DRT	3	rw	**Port 3 Disable Receive and Transmit**
P2DRT	2	rw	**Port 2 Disable Receive and Transmit**
P1DRT	1	rw	**Port 1 Disable Receive and Transmit**
P0DRT	0	rw	**Port 0 Disable Receive and Transmit** 0_B , The port acts as the normal mode. 1_B , The port will not receive or transmit packets. Learning is disabled in the disabled port.

Port Disable Register 1

PDR1	Offset	Reset Value
Port Disable Register 1	**$029F_H$**	**0000_H**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res						P25DRT	P24DRT	P23DRT	P22DRT	P21DRT	P20DRT	P19DRT	P18DRT	P17DRT	P16DRT
						rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
P25DRT	9	rw	**Port 25 Disable Receive and Transmit**
P24DRT	8	rw	**Port 24 Disable Receive and Transmit**
P23DRT	7	rw	**Port 23 Disable Receive and Transmit**
P22DRT	6	rw	**Port 22 Disable Receive and Transmit**

Field	Bits	Type	Description
P21DRT	5	rw	**Port 21 Disable Receive and Transmit**
P20DRT	4	rw	**Port 20 Disable Receive and Transmit**
P19DRT	3	rw	**Port 19 Disable Receive and Transmit**
P18DRT	2	rw	**Port 18 Disable Receive and Transmit**
P17DRT	1	rw	**Port 17 Disable Receive and Transmit**
P16DRT	0	rw	**Port 16 Disable Receive and Transmit**

IGMP Snooping Control Register 0

IGMPSCR0	Offset	Reset Value
IGMP Snooping Control Register 0	$02A0_H$	0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P15EISF	P14EISF	P13EISF	P12EISF	P11EISF	P10EISF	P9EISF	P8EISF	P7EISF	P6EISF	P5EISF	P4EISF	P3EISF	P2EISF	P1EISF	P0EISF
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
P15EISF	15	rw	**Port 15 Enable IGMP Snooping Function**
P14EISF	14	rw	**Port 14 Enable IGMP Snooping Function**
P13EISF	13	rw	**Port 13 Enable IGMP Snooping Function**
P12EISF	12	rw	**Port 12 Enable IGMP Snooping Function**
P11EISF	11	rw	**Port 11 Enable IGMP Snooping Function**
P10EISF	10	rw	**Port 10 Enable IGMP Snooping Function**
P9EISF	9	rw	**Port 9 Enable IGMP Snooping Function**
P8EISF	8	rw	**Port 8 Enable IGMP Snooping Function**
P7EISF	7	rw	**Port 7 Enable IGMP Snooping Function**
P6EISF	6	rw	**Port 6 Enable IGMP Snooping Function**
P5EISF	5	rw	**Port 5 Enable IGMP Snooping Function**
P4EISF	4	rw	**Port 4 Enable IGMP Snooping Function**
P3EISF	3	rw	**Port 3 Enable IGMP Snooping Function**
P2EISF	2	rw	**Port 2 Enable IGMP Snooping Function**
P1EISF	1	rw	**Port 1 Enable IGMP Snooping Function**
P0EISF	0	rw	**Port 0 Enable IGMP Snooping Function** The packets with the header (DA = 01005exxxxxx, Length_Type = 0800, IP version = 4, and Protocol type = 2) will be recognized as the IGMP packets, and the switch will forward it to the CPU port. 0_B , The port 0 is not configured to enable IGMP Snooping Function. And the IGMP packets will be handled as the normal multicast packets. 1_B , The port 0 is configured to enable IGMP Snooping Function.

IGMP Snooping Control Register 1

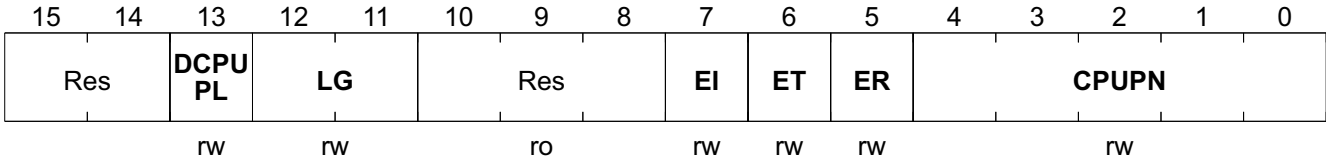
IGMPSCR1	Offset	Reset Value
IGMP Snooping Control Register 1	$02A1_H$	0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res				MCR		P25EISF	P24EISF	P23EISF	P22EISF	P21EISF	P20EISF	P19EISF	P18EISF	P17EISF	P16EISF
				rw		rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
MCR	11:10	rw	**Multicast Control Register** Packets with the following conditions will follow the Multicast Control Register to handle packets. Conditions: Destination address is not found in the address table. AND Destination address is a multicast address. AND Destination address is not all 1'b1. AND Destination address is not a reserved address(0180c2000~~). OR IGMP packets received by the port which disables the IGMP function. Multicast Control, Action 00_B , Forward to all ports within the same forwarding group except the self port. 01_B , Send to the CPU port. 10_B , Discard. 11_B , Reserved.
P25EISF	9	rw	**Port 25 Enable IGMP Snooping Function**
P24EISF	8	rw	**Port 24 Enable IGMP Snooping Function**
P23EISF	7	rw	**Port 23 Enable IGMP Snooping Function**
P22EISF	6	rw	**Port 22 Enable IGMP Snooping Function**
P21EISF	5	rw	**Port 21 Enable IGMP Snooping Function**
P20EISF	4	rw	**Port 20 Enable IGMP Snooping Function**
P19EISF	3	rw	**Port 19 Enable IGMP Snooping Function**
P18EISF	2	rw	**Port 18 Enable IGMP Snooping Function**
P17EISF	1	rw	**Port 17 Enable IGMP Snooping Function**
P16EISF	0	rw	**Port 16 Enable IGMP Snooping Function**

CPU Control Register

CPUCR	Offset	Reset Value
CPU Control Register	$02A2_H$	$001F_H$



Field	Bits	Type	Description
DCPUPL	13	rw	**Disable CPU Port Learning Function** 0_B , The packets received from the CPU port will be learned. 1_B , The packets received from the CPU port will not be learned.
LG	12:11	rw	**Learning Group** ADM6926/X has an ability to learn packets according their forwarding groups. The ADM6926/X could be divided into 32 learning groups. We use L0, L1, … and L31 to call each learning group. $0x_B$, Normal mode, learning with SA only. 10_B , MAC Clone mode, learning with SA and VID[0]. When packets are received and could be learned, they are learned divided into two Groups. Even forwarding groups are learned into L0 and odd forwarding groups are learned into L1. 11_B , Learning with SA and VID[4:0]. When packets are received and could be learned, they are learned according to their forwarding group. That is packets belonging to F0 is learned into L0, packets belonging to F1 is learned into L1, … and packets belonging to F31 is leaned into L31.
Res	10:8	ro	**Reserved**
EI	7	rw	**Enable Insert** Enable insert 4-byte special tag when Pause happens and Bit[6] is enabled. 0_B , ADM6926/X will add 4-byte special TAG when pause happens. 1_B , ADM6926/X will add 4-byte special TAG when pause happens.
ET	6	rw	**Enable Transmit** Enable transmit 4-byte special tag to the CPU port to support IGMP snooping, spanning tree or the security function. 0_B , ADM6926/X will transmit packets as the normal mode. 1_B , ADM6926/X will insert addition 4-byte special TAG when it has packets to be transmitted to the CPU port.
ER	5	rw	**Enable Receive** Enable receive 8-byte special tag from the CPU port to support IGMP snooping, spanning tree or the security function. 0_B , CPU will transmit packets as the normal state. 1_B , CPU will transmit packets with additional 8-byte special TAG and the ADM6926/X will remove this special TAG, use information contained to forward packets and recalculate CRC value when this packet is re-transmitted.

Field	Bits	Type	Description
CPUPN	4:0	rw	**CPU Port Number** The ADM6926/X allows any port to be configured to be the CPU port. The default CPU port is port 31. That is CPU port is not present. 00000_B , CPU port is configured to port 0. 00001_B , CPU port is configured to port 1. 00010_B , CPU port is configured to port 2. 00011_B , CPU port is configured to port 3. 00100_B , CPU port is configured to port 4. 00101_B , CPU port is configured to port 5. 00110_B , CPU port is configured to port 6. 00111_B , CPU port is configured to port 7. 01000_B , CPU port is configured to port 8. 01001_B , CPU port is configured to port 9. 01010_B , CPU port is configured to port 10. 01011_B , CPU port is configured to port 11. 01100_B , CPU port is configured to port 12. 01101_B , CPU port is configured to port 13. 01110_B , CPU port is configured to port 14. 01111_B , CPU port is configured to port 15. 10000_B , CPU port is configured to port 16. 10001_B , CPU port is configured to port 17. 10010_B , CPU port is configured to port 18. 10011_B , CPU port is configured to port 19. 10100_B , CPU port is configured to port 20. 10101_B , CPU port is configured to port 21. 10110_B , CPU port is configured to port 22. 10111_B , CPU port is configured to port 23. 11000_B , CPU port is configured to port 24. 11001_B , CPU port is configured to port 25.

Special MAC Forward Control Register 0

SMACFCR0	Offset	Reset Value
Special MAC Forward Control Register 0	$02A3_H$	0004_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F15_14		F13_12		F11_10		F9_8		F7_6		F5_4		F3_2		F1_0	
rw		rw		rw		rw		rw		rw		rw		rw	

Field	Bits	Type	Description
F15_14	15:14	rw	**Forwarding 15_14** The forwarding option for destination address = 0180c2000023 ~0180c20000ff

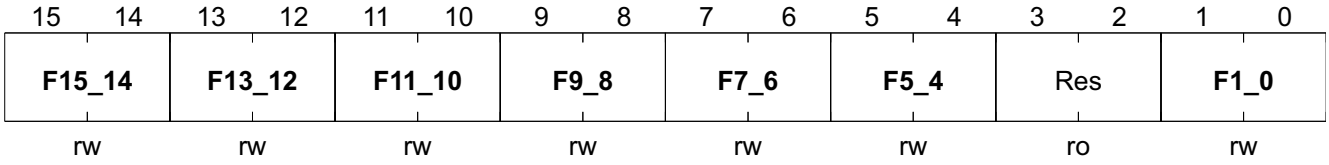
Field	Bits	Type	Description
F13_12	13:12	rw	**Forwarding 13_12** The forwarding option for destination address = 0180c2000020 ~0180c2000022 (GMRP, GVRP, GARP)
F11_10	11:10	rw	**Forwarding 11_10** The forwarding option for destination address = 0180c2000010 ~0180c200001f
F9_8	9:8	rw	**Forwarding 9_8** The forwarding option for destination address = 0180c2000004 ~0180c200000f
F7_6	7:6	rw	**Forwarding 7_6** The forwarding option for destination address = 0180c2000003 (802.1x PAE address)
F5_4	5:4	rw	**Forwarding 5_4** The forwarding option for destination address = 48'h0180c2000002 (Slow Protocol)
F3_2	3:2	rw	**Forwarding 3_2** The forwarding option for destination address = 0180c2000001 (Reserved for Pause address), MAC control field = 8808, OP Code!= 0001
F1_0	1:0	rw	**Forwarding 1_0** The forwarding option for destination address = 48'h0180c2000000 (BPDU)

Notes

1. *The options are defined here: 00_B = The switch will forward the packets as the normal mode. That is for reserved addresses existed in the learning table (because reserved address is multicast address, it could only be created through the CPU help if it really exists in the learning table). We will use "output port field" as the index to lookup the multicast table. At last, the looked output port map (may be modified by the forwarding process) is used as the output ports to forward packets. For reserved addresses, which don't exist in the learning table, it will be broadcast to the forwarding group except the receiving port.01_B = The switch will discard the packets.10_B = The switch will forward the packets to the CPU port. If the packet is received from the CPU port, the packet will be forwarded as the normal mode.11_B = The switch will forward the packet to CPU port. If this packet is received from CPU Port, this packet will be discard.*
2. *The forwarding options stated above will be of no effect for the CPU port when users enable the "Special Tag Function" and its output vector field is valid.*

Special MAC Forward Control Register 1

SMACFCR1	Offset	Reset Value
Special MAC Forward Control Register 1	**$02A4_H$**	**0003_H**



Field	Bits	Type	Description
F15_14	15:14	rw	**Forwarding 15_14** The forwarding option for destination address = 0180c2000023 ~0180c20000ff
F13_12	13:12	rw	**Forwarding 13_12** The forwarding option for destination address = 0180c2000020 ~0180c2000022 (GMRP, GVRP, GARP)
F11_10	11:10	rw	**Forwarding 11_10** The forwarding option for destination address = 0180c2000010 ~0180c200001f
F9_8	9:8	rw	**Forwarding 9_8** The forwarding option for destination address = 0180c2000004 ~0180c200000f
F7_6	7:6	rw	**Forwarding 7_6** The forwarding option for destination address = 0180c2000003 (802.1x PAE address)
F5_4	5:4	rw	**Forwarding 5_4** The forwarding option for destination address = 48'h0180c2000002 (Slow Protocol)
Res	3:2	ro	**Reserved**
F1_0	1:0	rw	**Forwarding 1_0** The forwarding option for destination address = 48'h0180c2000000 (BPDU)

Note: The ADM6926/X will divide packets into management or unmanagement packets. Management packets will not be dropped even if the buffer is full for no flow control environment. Only management packets will be forwarded or received in Blocking-N-Listening or the Learning state.
The options are defined here:00_B = The packets will not be classified as the management packets and it will be treated as the normal packet.01_B = The packets will be classified as the management packets and it will be transmitted no modified.10_B = The packets will be classified as the management packets and it will be transmitted without tag.11_B = The packets will be classified as the management packets and it will be transmitted with tag or without tag as the system configuration.

Special MAC Forward Control Register 2

SMACFCR2	Offset	Reset Value
Special MAC Forward Control Register 2	**$02A5_H$**	**0000_H**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res								**F7**	**F6**	**F5**	**F4**	**F3**	**F2**	Res	**F0**
								rw	rw	rw	rw	rw	rw	ro	rw

Field	Bits	Type	Description
F7	7	rw	**Forwarding 7** The forwarding option for destination address = 0180c2000023 ~0180c20000ff
F6	6	rw	**Forwarding 6** The forwarding option for destination address = 0180c2000020 ~0180c2000022 (GMRP, GVRP, GARP)
F5	5	rw	**Forwarding 5** The forwarding option for destination address = 0180c2000010 ~0180c200001f
F4	4	rw	**Forwarding 4** The forwarding option for destination address = 0180c2000004 ~0180c200000f
F3	3	rw	**Forwarding 3** The forwarding option for destination address = 0180c2000003 (802.1x PAE address)
F2	2	rw	**Forwarding 2** The forwarding option for destination address = 48'h0180c2000002 (Slow Protocol)
Res	1	ro	**Reserved**
F0	0	rw	**Forwarding 0** The forwarding option for destination address = 48'h0180c2000000 (BPDU)

Note: The options are defined here:1_B = The packets will cross forwarding group.0_B = The packets will not cross the forwarding packet.

Trunking Enable Register 0

TER0	**Offset**	**Reset Value**
Trunking Enable Register 0	**$02A6_H$**	**0000_H**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P15TE	**P14TE**	**P13TE**	**P12TE**	**P11TE**	**P10TE**	**P9TE**	**P8TE**	**P7TE**	**P6TE**	**P5TE**	**P4TE**	**P3TE**	**P2TE**	**P1TE**	**P0TE**
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
P15TE	15	rw	**Port 15 Trunking Enable**
P14TE	14	rw	**Port 14 Trunking Enable**
P13TE	13	rw	**Port 13 Trunking Enable**
P12TE	12	rw	**Port 12 Trunking Enable**
P11TE	11	rw	**Port 11 Trunking Enable**
P10TE	10	rw	**Port 10 Trunking Enable**
P9TE	9	rw	**Port 9 Trunking Enable**
P8TE	8	rw	**Port 8 Trunking Enable**
P7TE	7	rw	**Port 7 Trunking Enable**
P6TE	6	rw	**Port 6 Trunking Enable**
P5TE	5	rw	**Port 5 Trunking Enable**
P4TE	4	rw	**Port 4 Trunking Enable**
P3TE	3	rw	**Port 3 Trunking Enable**
P2TE	2	rw	**Port 2 Trunking Enable**
P1TE	1	rw	**Port 1 Trunking Enable**
P0TE	0	rw	**Port 0 Trunking Enable** The ADM6926/X supports one trunking port. Any port could be assigned to the trunking port. The trunking function is of the effect only the trunking hardware setting = 1. 0_B , Port 0 is not assigned to a member of the trunking port. 1_B , Port 0 is assigned to a member of the trunking port.

Trunking Enable Register 1

TER1	Offset	Reset Value
Trunking Enable Register 1	**$02A7_H$**	**0000_H**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res						P25TE	P24TE	P23TE	P22TE	P21TE	P20TE	P19TE	P18TE	P17TE	P16TE
						rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
P25TE	9	rw	**Port 25 Trunking Enable**
P24TE	8	rw	**Port 24 Trunking Enable**
P23TE	7	rw	**Port 23 Trunking Enable**
P22TE	6	rw	**Port 22 Trunking Enable**
P21TE	5	rw	**Port 21 Trunking Enable**
P20TE	4	rw	**Port 20 Trunking Enable**
P19TE	3	rw	**Port 19 Trunking Enable**

Field	Bits	Type	Description
P18TE	2	rw	**Port 18 Trunking Enable**
P17TE	1	rw	**Port 17 Trunking Enable**
P16TE	0	rw	**Port 16 Trunking Enable**

3.3 Switch Register Map

Table 25 Switch Register Map

Offset Hex	Bit 31 ~ 0	Type
0_H	Version ID	ro
1_H	Link Status	ro
2_H	Speed Status	ro
3_H	Duplex Status	ro
4_H	Flow Control Status	ro
5_H	Address Table Control Register 0	rw
6_H	Address Table Control Register 1	rw
7_H	Address Table Control Register 2	rw
8_H	Address Table Status Register 0	ro
9_H	Address Table Status Register 1	ro
A_H	Address Table Status Register 2	ro
B_H	PHY Control/Status Register	rw
C_H	Reserved	ro
D_H	Hardware Status	ro
E_H	RxPKT Overflow	roc
F_H	RxLEN Overflow	roc
10_H	TxPKT Overflow	roc
11_H	TxLEN Overflow	roc
12_H	RxERR Overflow	roc
13_H	RxCOL Overflow	roc
14_H	Renew Counter Register	rw
15_H	Read Counter Control Register	rw
16_H	Read Counter Status Register	ro
17_H	Reload MDIO Register	rw
18_H	P0 ~ P15 Spanning Tree Port State	rw
19_H	P16 ~ P25 Spanning Tree Port State	rw
$1A_H$	Source Port Register	ro
$1B_H$	Transmit Port Register	rw
$1C_H$	Buffer Status Register 0	roc
$1D_H$	Buffer Status Register 1	roc
$1E_H$	Buffer Status Register 2	roc
$1F_H$	Buffer Status Register 3	roc

Table 25 Switch Register Map (cont'd)

Offset Hex	Bit 31 ~ 0	Type
$1xx_H$	Counter Register	rw
$2xx_H$	EEPROM Register	rw

3.3.1 Switch Registers Overview

Table 26 Registers Address Space

Module	Base Address	End Address	Note
Switch	00_H	$1B_H$	

Table 27 Registers Overview

Register Short Name	Register Long Name	Offset Address	Page Number
VID	Version ID	00_H	93
LS	Link Status	01_H	94
SS	Speed Status	02_H	95
DS	Duplex Status	03_H	96
FCS	Flow Control Status	04_H	97
PHYCR	PHY Control Register	$0B_H$	98
HS	Hardware Status	$0D_H$	99
RPCO	Receive Packet Count Overflow	$0E_H$	99
RPLCO	Receive Packet Length Count Overflow	$0F_H$	100
TPCO	Transmit Packet Count Overflow	10_H	101
TPLCO	Transmit Packet Length Count Overflow	11_H	102
ECO	Error Count Overflow	12_H	103
CCO	Collision Count Overflow	13_H	104
RCR	Renew Counter Register	14_H	105
RCCR	Read Counter Control Register	15_H	107
RCSR	Read Counter Status Register	16_H	108
RMDIOR	Reload MDIO Register	17_H	108
STPS0	Spanning Tree Port State 0	18_H	109
STPS1	Spanning Tree Port State 1	19_H	110
SCPR	Source Port Register	$1A_H$	111
TRPR	Transmit Port Register	$1B_H$	111

The register is addressed wordwise.

Table 28 Register Access Types

Mode	Symbol	Description HW	Description SW
read/write	rw	Register is used as input for the HW	Register is read and writable by SW
read	r	Register is written by HW (register between input and output -> one cycle delay)	Value written by software is ignored by hardware; that is, software may write any value to this field without affecting hardware behavior (= Target for development.)
Read only	ro	Register is set by HW (register between input and output -> one cycle delay)	SW can only read this register

Table 28 Register Access Types (cont'd)

Mode	Symbol	Description HW	Description SW
Read virtual	rv	Physically, there is no new register, the input of the signal is connected directly to the address multiplexer.	SW can only read this register
Latch high, self clearing	lhsc	Latch high signal at high level, clear on read	SW can read the register
Latch low, self clearing	llsc	Latch high signal at low-level, clear on read	SW can read the register
Latch high, mask clearing	lhmk	Latch high signal at high level, register cleared with written mask	SW can read the register, with write mask the register can be cleared (1 clears)
Latch low, mask clearing	llmk	Latch high signal at low-level, register cleared on read	SW can read the register, with write mask the register can be cleared (1 clears)
Interrupt high, self clearing	ihsc	Differentiate the input signal (low->high) register cleared on read	SW can read the register
Interrupt low, self clearing	ilsc	Differentiate the input signal (high->low) register cleared on read	SW can read the register
Interrupt high, mask clearing	ihmk	Differentiate the input signal (high->low) register cleared with written mask	SW can read the register, with write mask the register can be cleared
Interrupt low, mask clearing	ilmk	Differentiate the input signal (low->high) register cleared with written mask	SW can read the register, with write mask the register can be cleared
Interrupt enable register	ien	Enables the interrupt source for interrupt generation	SW can read and write this register
latch_on_reset	lor	rw register, value is latched after first clock cycle after reset	Register is read and writable by SW
Read/write self clearing	rwsc	Register is used as input for the hw, the register will be cleared due to a HW mechanism.	Writing to the register generates a strobe signal for the HW (1 pdi clock cycle) Register is read and writable by SW.

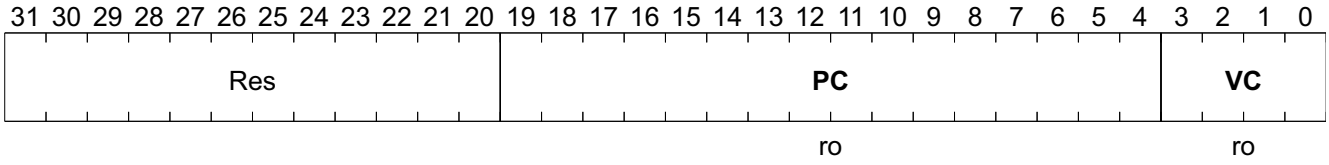
Table 29 Registers Clock DomainsRegisters Clock Domains

Clock Short Name	Description

3.3.1.1 Switch Registers Descriptions

Version ID

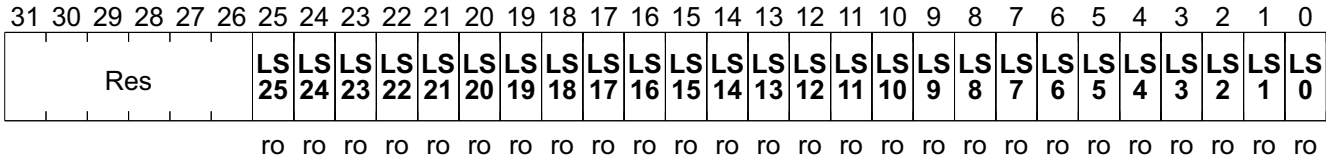
VID	Offset	Reset Value
Version ID	00_H	$0003\ 1101_H$



Field	Bits	Type	Description
PC	19:4	ro	**Project Code**
VC	3:0	ro	**Version Code**

Link Status

LS	Offset	Reset Value
Link Status	**01_H**	**$03FF\ FFFF_H$**



Field	Bits	Type	Description
LS25	25	ro	**Port 25 Link Status**
LS24	24	ro	**Port 24 Link Status**
LS23	23	ro	**Port 23 Link Status**
LS22	22	ro	**Port 22 Link Status**
LS21	21	ro	**Port 21 Link Status**
LS20	20	ro	**Port 20 Link Status**
LS19	19	ro	**Port 19 Link Status**
LS18	18	ro	**Port 18 Link Status**
LS17	17	ro	**Port 17 Link Status**
LS16	16	ro	**Port 16 Link Status**
LS15	15	ro	**Port 15 Link Status**
LS14	14	ro	**Port 14 Link Status**
LS13	13	ro	**Port 13 Link Status**
LS12	12	ro	**Port 12 Link Status**
LS11	11	ro	**Port 11 Link Status**
LS10	10	ro	**Port 10 Link Status**
LS9	9	ro	**Port 9 Link Status**
LS8	8	ro	**Port 8 Link Status**
LS7	7	ro	**Port 7 Link Status**
LS6	6	ro	**Port 6 Link Status**
LS5	5	ro	**Port 5 Link Status**

Field	Bits	Type	Description
LS4	4	ro	**Port 4 Link Status**
LS3	3	ro	**Port 3 Link Status**
LS2	2	ro	**Port 2 Link Status**
LS1	1	ro	**Port 1 Link Status**
LS0	0	ro	**Port 0 Link Status** 0_B , Port 0 links down. 1_B , Port 0 links up.

Speed Status

SS	Offset	Reset Value
Speed Status	**02_H**	**$03FF\ FFFF_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res						SS25	SS24	SS23	SS22	SS21	SS20	SS19	SS18	SS17	SS16	SS15	SS14	SS13	SS12	SS11	SS10	SS9	SS8	SS7	SS6	SS5	SS	SS3	SS2	SS1	SS0
						ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro

Field	Bits	Type	Description
SS25	25	ro	**Port 25 Speed Status**
SS24	24	ro	**Port 24 Speed Status**
SS23	23	ro	**Port 23 Speed Status**
SS22	22	ro	**Port 22 Speed Status**
SS21	21	ro	**Port 21 Speed Status**
SS20	20	ro	**Port 20 Speed Status**
SS19	19	ro	**Port 19 Speed Status**
SS18	18	ro	**Port 18 Speed Status**
SS17	17	ro	**Port 17 Speed Status**
SS16	16	ro	**Port 16 Speed Status**
SS15	15	ro	**Port 15 Speed Status**
SS14	14	ro	**Port 14 Speed Status**
SS13	13	ro	**Port 13 Speed Status**
SS12	12	ro	**Port 12 Speed Status**
SS11	11	ro	**Port 11 Speed Status**
SS10	10	ro	**Port 10 Speed Status**
SS9	9	ro	**Port 9 Speed Status**
SS8	8	ro	**Port 8 Speed Status**
SS7	7	ro	**Port 7 Speed Status**
SS6	6	ro	**Port 6 Speed Status**
SS5	5	ro	**Port 5 Speed Status**
SS	4	ro	**Port 4 Speed Status**

Field	Bits	Type	Description
SS3	3	ro	**Port 3 Speed Status**
SS2	2	ro	**Port 2 Speed Status**
SS1	1	ro	**Port 1 Speed Status**
SS0	0	ro	**Port 0 Speed Status** 0_B , Port 0 operates in 10M. 1_B , Port 0 operates in 100M.

Duplex Status

DS	Offset	Reset Value
Duplex Status	**03_H**	**$03FF\ FFFF_H$**

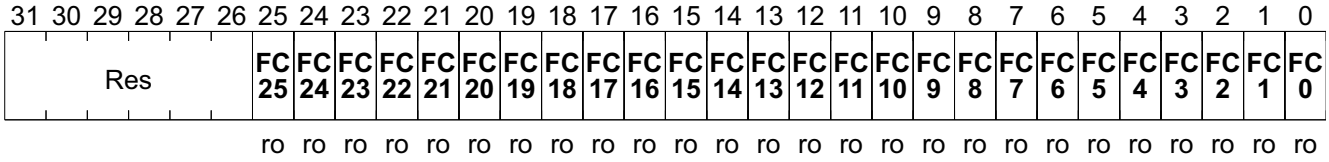
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res						**DS25**	**DS24**	**DS23**	**DS22**	**DS21**	**DS20**	**DS19**	**DS18**	**DS17**	**DS16**	**DS15**	**DS14**	**DS13**	**DS12**	**DS11**	**DS10**	**DS9**	**DS8**	**DS7**	**DS6**	**DS5**	**DS4**	**DS3**	**DS2**	**DS1**	**DS0**
						ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro

Field	Bits	Type	Description
DS25	25	ro	**Port 25 Duplex Status**
DS24	24	ro	**Port 24 Duplex Status**
DS23	23	ro	**Port 23 Duplex Status**
DS22	22	ro	**Port 22 Duplex Status**
DS21	21	ro	**Port 21 Duplex Status**
DS20	20	ro	**Port 20 Duplex Status**
DS19	19	ro	**Port 19 Duplex Status**
DS18	18	ro	**Port 18 Duplex Status**
DS17	17	ro	**Port 17 Duplex Status**
DS16	16	ro	**Port 16 Duplex Status**
DS15	15	ro	**Port 15 Duplex Status**
DS14	14	ro	**Port 14 Duplex Status**
DS13	13	ro	**Port 13 Duplex Status**
DS12	12	ro	**Port 12 Duplex Status**
DS11	11	ro	**Port 11 Duplex Status**
DS10	10	ro	**Port 10 Duplex Status**
DS9	9	ro	**Port 9 Duplex Status**
DS8	8	ro	**Port 8 Duplex Status**
DS7	7	ro	**Port 7 Duplex Status**
DS6	6	ro	**Port 6 Duplex Status**
DS5	5	ro	**Port 5 Duplex Status**
DS4	4	ro	**Port 4 Duplex Status**
DS3	3	ro	**Port 3 Duplex Status**

Field	Bits	Type	Description
DS2	2	ro	**Port 2 Duplex Status**
DS1	1	ro	**Port 1 Duplex Status**
DS0	0	ro	**Port 0 Duplex Status** 0_B , Port 0 operates in half duplex. 1_B , Port 0 operates in full duplex.

Flow Control Status

FCS	Offset	Reset Value
Flow Control Status	**04_H**	**$03FF\ FFFF_H$**

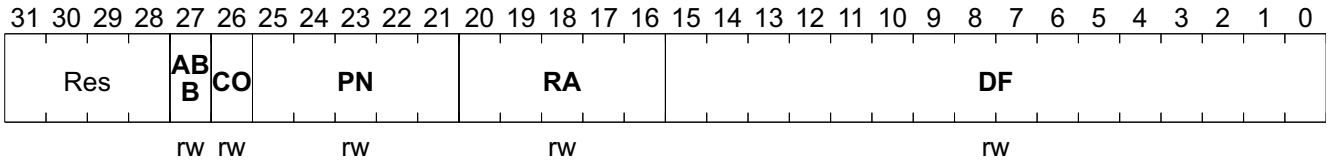


Field	Bits	Type	Description
FC25	25	ro	**Port 25 Flow Control Status**
FC24	24	ro	**Port 24 Flow Control Status**
FC23	23	ro	**Port 23 Flow Control Status**
FC22	22	ro	**Port 22 Flow Control Status**
FC21	21	ro	**Port 21 Flow Control Status**
FC20	20	ro	**Port 20 Flow Control Status**
FC19	19	ro	**Port 19 Flow Control Status**
FC18	18	ro	**Port 18 Flow Control Status**
FC17	17	ro	**Port 17 Flow Control Status**
FC16	16	ro	**Port 16 Flow Control Status**
FC15	15	ro	**Port 15 Flow Control Status**
FC14	14	ro	**Port 14 Flow Control Status**
FC13	13	ro	**Port 13 Flow Control Status**
FC12	12	ro	**Port 12 Flow Control Status**
FC11	11	ro	**Port 11 Flow Control Status**
FC10	10	ro	**Port 10 Flow Control Status**
FC9	9	ro	**Port 9 Flow Control Status**
FC8	8	ro	**Port 8 Flow Control Status**
FC7	7	ro	**Port 7 Flow Control Status**
FC6	6	ro	**Port 6 Flow Control Status**
FC5	5	ro	**Port 5 Flow Control Status**
FC4	4	ro	**Port 4 Flow Control Status**
FC3	3	ro	**Port 3 Flow Control Status**
FC2	2	ro	**Port 2 Flow Control Status**

Field	Bits	Type	Description
FC1	1	ro	**Port 1 Flow Control Status**
FC0	0	ro	**Port 0 Flow Control Status** 0_B , Port 0 disables flow control function. 1_B , Port 0 enables Pause function in full duplex or Back Pressure function in half duplex.

PHY Control Register

PHYCR	Offset	Reset Value
PHY Control Register	$0B_H$	$0000\ 0000_H$



Field	Bits	Type	Description
ABB	27	rw	**Access (Busy) Bit**
CO	26	rw	**Command Option** 0_B , Write 1_B , Read
PN	25:21	rw	**Port Number**
RA	20:16	rw	**Register Address**
DF	15:0	rw	**Data Field** This field indicates the data for reading or writing.

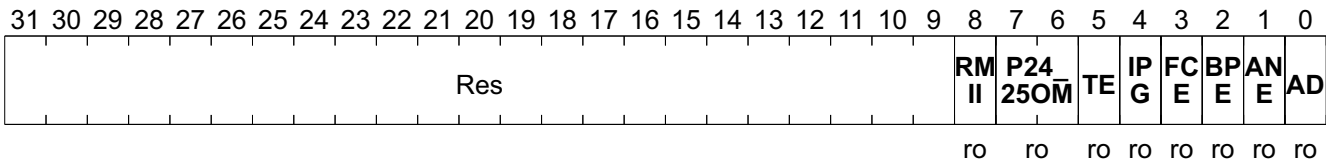
Notes

1. *This register allows the user to control the PHY attached through the CUP's help.*
2. *Rule for Read Operation:*
   Step 1: Poll the Busy bit (Bit[27]) to check if the PHY control module is busy.
   Step 2: Write the port number (Bit[25:21]), register address (Bit[20:16]), command (Bit[26]) and Access bit(Bit[27]) to start the read operation.
   Step 3: Poll the Busy bit (Bit[27]). If Busy = 1'b1, wait. If Busy = 1'b0, data is returned in the data field.
3. *Rule for Write Operation:*
   Step 1: Poll the Busy bit (Bit[27]) to check if the PHY control module is busy.
   Step 2: Write the port number (Bit[25:21]), register address (Bit[20:16]), command (Bit[26]), data field (Bit[15:0]) and Access bit(Bit[27]) to start the write operation.
   Step 3: Poll the Busy bit (Bit[27]). If Busy = 1'b1, wait. If Busy = 1'b0, writing operation completes.
4. *Example: The user wants to read the Basic Control Register in Port 1.*
   Step 1: Read Bit[27] to check if PHY module is in progress.
   Step 2: If Bit[27] = 1'b0, write Bit[27] = 1'b1, Bit[26] = 1'b1, Bit[25:21] = 5'h1 and Bit[20:16] = 5'h0.
   Step 3: Poll the Busy bit. If Bit[27] = 1'b0, data is returned in the data field. If Bit[27] = 1'b1, wait.

Hardware Status

The Reset Value is done by hardware setting.

HS	Offset	Reset Value
Hardware Status	$0D_H$	$_H$



Field	Bits	Type	Description
RMII	8	ro	**Bond RMII (SS-SMII or Pure RMII Mode)** 0_B , The switch is in SS-SMII package. 1_B , The switch is in RMII package.
P24_25OM	7:6	ro	**Port 24 or Port 25 Operate in RMII or MII Mode** 00_B , Port 24 and Port 25 are both configured to MII mode. 01_B , Port 24 is configured to RMII; Port 25 is configured to MII. 10_B , Port 24 is configured to MII; Port 25 is configured to RMII. 11_B , Port 24 and Port 25 are both configured to RMII.
TE	5	ro	**Trunking Enable From Hardware** 0_B , Trunking Disable. 1_B , Trunking Enable.
IPG	4	ro	**IPG 92 Bit Time Enable From Hardware Pin** 0_B , IPG 92 Disable. 1_B , IPG 92 Enable.
FCE	3	ro	**Flow Control Enable For Full Duplex From Hardware Pin** 0_B , Flow Control Disable. 1_B , Flow Control Enable.
BPE	2	ro	**Back Pressure Enable From Hardware Pin** 0_B , Back Pressure Disable. 1_B , Back Pressure Enable.
ANE	1	ro	**Auto-Negotiation Enable From Hardware Pin** 0_B , Auto-Negotiation Disable. 1_B , Auto-Negotiation Enable.
AD	0	ro	**Aging Disable From Hardware Pin** 0_B , Aging Enable. 1_B , Aging Disable.

Receive Packet Count Overflow

RPCO	Offset	Reset Value
Receive Packet Count Overflow	$0E_H$	$0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res						CO25	CO24	CO23	CO22	CO21	CO20	CO19	CO18	CO17	CO16	CO15	CO14	CO13	CO12	CO11	CO10	CO9	CO8	CO7	CO6	CO5	CO4	CO3	CO2	CO1	CO0
						roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc

Field	Bits	Type	Description
CO25	25	roc	**Port 25 Receive Packet Count Overflow**
CO24	24	roc	**Port 24 Receive Packet Count Overflow**
CO23	23	roc	**Port 23 Receive Packet Count Overflow**
CO22	22	roc	**Port 22 Receive Packet Count Overflow**
CO21	21	roc	**Port 21 Receive Packet Count Overflow**
CO20	20	roc	**Port 20 Receive Packet Count Overflow**
CO19	19	roc	**Port 19 Receive Packet Count Overflow**
CO18	18	roc	**Port 18 Receive Packet Count Overflow**
CO17	17	roc	**Port 17 Receive Packet Count Overflow**
CO16	16	roc	**Port 16 Receive Packet Count Overflow**
CO15	15	roc	**Port 15 Receive Packet Count Overflow**
CO14	14	roc	**Port 14 Receive Packet Count Overflow**
CO13	13	roc	**Port 13 Receive Packet Count Overflow**
CO12	12	roc	**Port 12 Receive Packet Count Overflow**
CO11	11	roc	**Port 11 Receive Packet Count Overflow**
CO10	10	roc	**Port 10 Receive Packet Count Overflow**
CO9	9	roc	**Port 9 Receive Packet Count Overflow**
CO8	8	roc	**Port 8 Receive Packet Count Overflow**
CO7	7	roc	**Port 7 Receive Packet Count Overflow**
CO6	6	roc	**Port 6 Receive Packet Count Overflow**
CO5	5	roc	**Port 5 Receive Packet Count Overflow**
CO4	4	roc	**Port 4 Receive Packet Count Overflow**
CO3	3	roc	**Port 3 Receive Packet Count Overflow**
CO2	2	roc	**Port 2 Receive Packet Count Overflow**
CO1	1	roc	**Port 1 Receive Packet Count Overflow**
CO0	0	roc	**Port 0 Receive Packet Count Overflow** 1_B , Receive packet count in port 0 overflows and it will be cleared after read from CPU.

Receive Packet Length Count Overflow

RPLCO	Offset	Reset Value
Receive Packet Length Count Overflow	**$0F_H$**	**$0000\ 0000_H$**

31 30 29 28 27 26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res	RL25	RL24	RL23	RL22	RL21	RL20	RL19	RL18	RL17	RL16	RL15	RL14	RL13	RL12	RL11	RL10	RL9	RL8	RL7	RL6	RL5	RL4	RL3	RL2	RL1	RL0
	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc

Field	Bits	Type	Description
RL25	25	roc	**Port 25 Receive Packet Length Count Overflow**
RL24	24	roc	**Port 24 Receive Packet Length Count Overflow**
RL23	23	roc	**Port 23 Receive Packet Length Count Overflow**
RL22	22	roc	**Port 22 Receive Packet Length Count Overflow**
RL21	21	roc	**Port 21 Receive Packet Length Count Overflow**
RL20	20	roc	**Port 20 Receive Packet Length Count Overflow**
RL19	19	roc	**Port 19 Receive Packet Length Count Overflow**
RL18	18	roc	**Port 18 Receive Packet Length Count Overflow**
RL17	17	roc	**Port 17 Receive Packet Length Count Overflow**
RL16	16	roc	**Port 16 Receive Packet Length Count Overflow**
RL15	15	roc	**Port 15 Receive Packet Length Count Overflow**
RL14	14	roc	**Port 14 Receive Packet Length Count Overflow**
RL13	13	roc	**Port 13 Receive Packet Length Count Overflow**
RL12	12	roc	**Port 12 Receive Packet Length Count Overflow**
RL11	11	roc	**Port 11 Receive Packet Length Count Overflow**
RL10	10	roc	**Port 10 Receive Packet Length Count Overflow**
RL9	9	roc	**Port 9 Receive Packet Length Count Overflow**
RL8	8	roc	**Port 8 Receive Packet Length Count Overflow**
RL7	7	roc	**Port 7 Receive Packet Length Count Overflow**
RL6	6	roc	**Port 6 Receive Packet Length Count Overflow**
RL5	5	roc	**Port 5 Receive Packet Length Count Overflow**
RL4	4	roc	**Port 4 Receive Packet Length Count Overflow**
RL3	3	roc	**Port 3 Receive Packet Length Count Overflow**
RL2	2	roc	**Port 2 Receive Packet Length Count Overflow**
RL1	1	roc	**Port 1 Receive Packet Length Count Overflow**
RL0	0	roc	**Port 0 Receive Packet Length Count Overflow** 1_B , Receive packet length count in port 0 overflows and it will be cleared after read from CPU.

Transmit Packet Count Overflow

TPCO	Offset	Reset Value
Transmit Packet Count Overflow	**10_H**	**$0000\ 0000_H$**

31 30 29 28 27 26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res	TP25	TP24	TP23	TP22	TP21	TP20	TP19	TP18	TP17	TP16	TP15	TP14	TP13	TP12	TP11	TP10	TP9	TP8	TP7	TP6	TP5	TP4	TP3	TP2	TP1	TP0
	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc

Field	Bits	Type	Description
TP25	25	roc	**Port 25 Transmit Packet Count Overflow**
TP24	24	roc	**Port 24 Transmit Packet Count Overflow**
TP23	23	roc	**Port 23 Transmit Packet Count Overflow**
TP22	22	roc	**Port 22 Transmit Packet Count Overflow**
TP21	21	roc	**Port 21 Transmit Packet Count Overflow**
TP20	20	roc	**Port 20 Transmit Packet Count Overflow**
TP19	19	roc	**Port 19 Transmit Packet Count Overflow**
TP18	18	roc	**Port 18 Transmit Packet Count Overflow**
TP17	17	roc	**Port 17 Transmit Packet Count Overflow**
TP16	16	roc	**Port 16 Transmit Packet Count Overflow**
TP15	15	roc	**Port 15 Transmit Packet Count Overflow**
TP14	14	roc	**Port 14 Transmit Packet Count Overflow**
TP13	13	roc	**Port 13 Transmit Packet Count Overflow**
TP12	12	roc	**Port 12 Transmit Packet Count Overflow**
TP11	11	roc	**Port 11 Transmit Packet Count Overflow**
TP10	10	roc	**Port 10 Transmit Packet Count Overflow**
TP9	9	roc	**Port 9 Transmit Packet Count Overflow**
TP8	8	roc	**Port 8 Transmit Packet Count Overflow**
TP7	7	roc	**Port 7 Transmit Packet Count Overflow**
TP6	6	roc	**Port 6 Transmit Packet Count Overflow**
TP5	5	roc	**Port 5 Transmit Packet Count Overflow**
TP4	4	roc	**Port 4 Transmit Packet Count Overflow**
TP3	3	roc	**Port 3 Transmit Packet Count Overflow**
TP2	2	roc	**Port 2 Transmit Packet Count Overflow**
TP1	1	roc	**Port 1 Transmit Packet Count Overflow**
TP0	0	roc	**Port 0 Transmit Packet Count Overflow** 1_B , Transmit packet count in port 0 overflows and it will be cleared after read from CPU.

Transmit Packet Length Count Overflow

TPLCO	Offset	Reset Value
Transmit Packet Length Count Overflow	**11_H**	**$0000\ 0000_H$**

31 30 29 28 27 26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res	TL25	TL24	TL23	TL22	TL21	TL20	TL19	TL18	TL17	TL16	TL15	TL14	TL13	TL12	TL11	TL10	TL9	TL8	TL7	TL6	TL5	TL4	TL3	TL2	TL1	TL0
	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc

Field	Bits	Type	Description
TL25	25	roc	**Port 25 Transmit Packet Length Count Overflow**
TL24	24	roc	**Port 24 Transmit Packet Length Count Overflow**
TL23	23	roc	**Port 23 Transmit Packet Length Count Overflow**
TL22	22	roc	**Port 22 Transmit Packet Length Count Overflow**
TL21	21	roc	**Port 21 Transmit Packet Length Count Overflow**
TL20	20	roc	**Port 20 Transmit Packet Length Count Overflow**
TL19	19	roc	**Port 19 Transmit Packet Length Count Overflow**
TL18	18	roc	**Port 18 Transmit Packet Length Count Overflow**
TL17	17	roc	**Port 17 Transmit Packet Length Count Overflow**
TL16	16	roc	**Port 16 Transmit Packet Length Count Overflow**
TL15	15	roc	**Port 15 Transmit Packet Length Count Overflow**
TL14	14	roc	**Port 14 Transmit Packet Length Count Overflow**
TL13	13	roc	**Port 13 Transmit Packet Length Count Overflow**
TL12	12	roc	**Port 12 Transmit Packet Length Count Overflow**
TL11	11	roc	**Port 11 Transmit Packet Length Count Overflow**
TL10	10	roc	**Port 10 Transmit Packet Length Count Overflow**
TL9	9	roc	**Port 9 Transmit Packet Length Count Overflow**
TL8	8	roc	**Port 8 Transmit Packet Length Count Overflow**
TL7	7	roc	**Port 7 Transmit Packet Length Count Overflow**
TL6	6	roc	**Port 6 Transmit Packet Length Count Overflow**
TL5	5	roc	**Port 5 Transmit Packet Length Count Overflow**
TL4	4	roc	**Port 4 Transmit Packet Length Count Overflow**
TL3	3	roc	**Port 3 Transmit Packet Length Count Overflow**
TL2	2	roc	**Port 2 Transmit Packet Length Count Overflow**
TL1	1	roc	**Port 1 Transmit Packet Length Count Overflow**
TL0	0	roc	**Port 0 Transmit Packet Length Count Overflow** 1_B , Transmit packet length count in port 0 overflows and it will be cleared after read from CPU.

Error Count Overflow

ECO	Offset	Reset Value
Error Count Overflow	**12_H**	**0000 0000$_H$**

31 30 29 28 27 26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res	EC25	EC24	EC23	EC22	EC21	EC20	EC19	EC18	EC17	EC16	EC15	EC14	EC13	EC12	EC11	EC10	EC9	EC8	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0
	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc

Field	Bits	Type	Description
EC25	25	roc	**Port 25 Error Count Overflow**
EC24	24	roc	**Port 24 Error Count Overflow**
EC23	23	roc	**Port 23 Error Count Overflow**
EC22	22	roc	**Port 22 Error Count Overflow**
EC21	21	roc	**Port 21 Error Count Overflow**
EC20	20	roc	**Port 20 Error Count Overflow**
EC19	19	roc	**Port 19 Error Count Overflow**
EC18	18	roc	**Port 18 Error Count Overflow**
EC17	17	roc	**Port 17 Error Count Overflow**
EC16	16	roc	**Port 16 Error Count Overflow**
EC15	15	roc	**Port 15 Error Count Overflow**
EC14	14	roc	**Port 14 Error Count Overflow**
EC13	13	roc	**Port 13 Error Count Overflow**
EC12	12	roc	**Port 12 Error Count Overflow**
EC11	11	roc	**Port 11 Error Count Overflow**
EC10	10	roc	**Port 10 Error Count Overflow**
EC9	9	roc	**Port 9 Error Count Overflow**
EC8	8	roc	**Port 8 Error Count Overflow**
EC7	7	roc	**Port 7 Error Count Overflow**
EC6	6	roc	**Port 6 Error Count Overflow**
EC5	5	roc	**Port 5 Error Count Overflow**
EC4	4	roc	**Port 4 Error Count Overflow**
EC3	3	roc	**Port 3 Error Count Overflow**
EC2	2	roc	**Port 2 Error Count Overflow**
EC1	1	roc	**Port 1 Error Count Overflow**
EC0	0	roc	**Port 0 Error Count Overflow** 1_B , Error count in port 0 overflows and it will be cleared after read from CPU.

Collision Count Overflow

CCO	Offset	Reset Value
Collision Count Overflow	**13_H**	**0000 0000$_H$**

31 30 29 28 27 26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res	CC25	CC24	CC23	CC22	CC21	CC20	CC19	CC18	CC17	CC16	CC15	CC14	CC13	CC12	CC11	CC10	CC9	CC8	CC7	CC6	CC5	CC4	CC3	CC2	CC1	CC0
	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc	roc

Field	Bits	Type	Description
CC25	25	roc	**Port 25 Collision Count Overflow**
CC24	24	roc	**Port 24 Collision Count Overflow**
CC23	23	roc	**Port 23 Collision Count Overflow**
CC22	22	roc	**Port 22 Collision Count Overflow**
CC21	21	roc	**Port 21 Collision Count Overflow**
CC20	20	roc	**Port 20 Collision Count Overflow**
CC19	19	roc	**Port 19 Collision Count Overflow**
CC18	18	roc	**Port 18 Collision Count Overflow**
CC17	17	roc	**Port 17 Collision Count Overflow**
CC16	16	roc	**Port 16 Collision Count Overflow**
CC15	15	roc	**Port 15 Collision Count Overflow**
CC14	14	roc	**Port 14 Collision Count Overflow**
CC13	13	roc	**Port 13 Collision Count Overflow**
CC12	12	roc	**Port 12 Collision Count Overflow**
CC11	11	roc	**Port 11 Collision Count Overflow**
CC10	10	roc	**Port 10 Collision Count Overflow**
CC9	9	roc	**Port 9 Collision Count Overflow**
CC8	8	roc	**Port 8 Collision Count Overflow**
CC7	7	roc	**Port 7 Collision Count Overflow**
CC6	6	roc	**Port 6 Collision Count Overflow**
CC5	5	roc	**Port 5 Collision Count Overflow**
CC4	4	roc	**Port 4 Collision Count Overflow**
CC3	3	roc	**Port 3 Collision Count Overflow**
CC2	2	roc	**Port 2 Collision Count Overflow**
CC1	1	roc	**Port 1 Collision Count Overflow**
CC0	0	roc	**Port 0 Collision Count Overflow** 1_B , Collision Count in port 0 overflows and it will be cleared after read from CPU.

Renew Counter Register

RCR	Offset	Reset Value
Renew Counter Register	**14_H**	**$0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res					ABB	C25	C24	C23	C22	C21	C20	C19	C18	C17	C16	C15	C14	C13	C12	C11	C10	C9	C8	C7	C6	C5	C4	C3	C2	C1	C0
					rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
ABB	26	rw	**Access (Busy) Bit**
C25	25	rw	**Counter Port 25** 1_B , Clear Port 25 Corresponding Counters
C24	24	rw	**Counter Port 24** 1_B , Clear Port 24 Corresponding Counters
C23	23	rw	**Counter Port 23** 1_B , Clear Port 23 Corresponding Counters
C22	22	rw	**Counter Port 22** 1_B , Clear Port 22 Corresponding Counters
C21	21	rw	**Counter Port 21** 1_B , Clear Port 21 Corresponding Counters
C20	20	rw	**Counter Port 20** 1_B , Clear Port 20 Corresponding Counters
C19	19	rw	**Counter Port 19** 1_B , Clear Port 19 Corresponding Counters
C18	18	rw	**Counter Port 18** 1_B , Clear Port 18 Corresponding Counters
C17	17	rw	**Counter Port 17** 1_B , Clear Port 17 Corresponding Counters
C16	16	rw	**Counter Port 16** 1_B , Clear Port 16 Corresponding Counters
C15	15	rw	**Counter Port 15** 1_B , Clear Port 15 Corresponding Counters
C14	14	rw	**Counter Port 14** 1_B , Clear Port 14 Corresponding Counters
C13	13	rw	**Counter Port 13** 1_B , Clear Port 13 Corresponding Counters
C12	12	rw	**Counter Port 12** 1_B , Clear Port 12 Corresponding Counters
C11	11	rw	**Counter Port 11** 1_B , Clear Port 11 Corresponding Counters
C10	10	rw	**Counter Port 10** 1_B , Clear Port 10 Corresponding Counters
C9	9	rw	**Counter Port 9** 1_B , Clear Port 9 Corresponding Counters
C8	8	rw	**Counter Port 8** 1_B , Clear Port 8 Corresponding Counters
C7	7	rw	**Counter Port 7** 1_B , Clear Port 7 Corresponding Counters

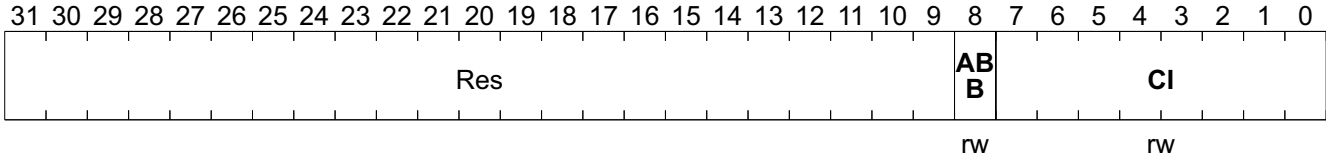
Field	Bits	Type	Description
C6	6	rw	**Counter Port 6** 1_B , Clear Port 6 Corresponding Counters
C5	5	rw	**Counter Port 5** 1_B , Clear Port 5 Corresponding Counters
C4	4	rw	**Counter Port 4** 1_B , Clear Port 4 Corresponding Counters
C3	3	rw	**Counter Port 3** 1_B , Clear Port 3 Corresponding Counters
C2	2	rw	**Counter Port 2** 1_B , Clear Port 2 Corresponding Counters
C1	1	rw	**Counter Port 1** 1_B , Clear Port 1 Corresponding Counters
C0	0	rw	**Counter Port 0** 1_B , Clear Port 0 Corresponding Counters

Notes

1. *This register allows the user to reset all counters for the corresponding port. If the renew counter module is busy all other modules about counters are not accessible.*
2. *Rule:*
   Step 1: Poll the busy bit to check if the renew counter module is busy.
   Step 2: If the renew counter module is available, write the port (Bit[25:0]) the user wants to reset and the busy bit(Bit[26]) to 1.
   Step 3: Poll the busy bit to check if the renew counter module completes the job.
3. *Example:*
   Users want to reset P0, P1, P2, P3 corresponding counters.
   Step 1: Read Bit[26] to check if reset is in progress.
   Step 2: If Bit[26] = 0, write Bit[26] = 1'b1, Bit[25:0] = 26'b00_0000_0000_0000_0000_0000_1111 into the register.
   Step 3: Poll the busy bit to check if reset completes.

Read Counter Control Register

RCCR	Offset	Reset Value
Read Counter Control Register	**15_H**	**0000_0000_H**

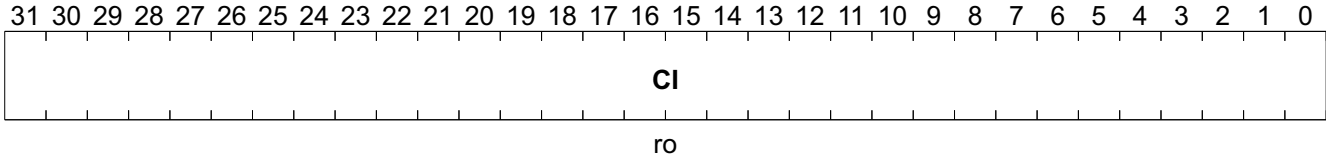


Field	Bits	Type	Description
ABB	8	rw	**Access (Busy) Bit**

Field	Bits	Type	Description
CI	7:0	rw	**Counter Index**

Read Counter Status Register

RCSR	Offset	Reset Value
Read Counter Status Register	**16_H**	**0000 0000_H**



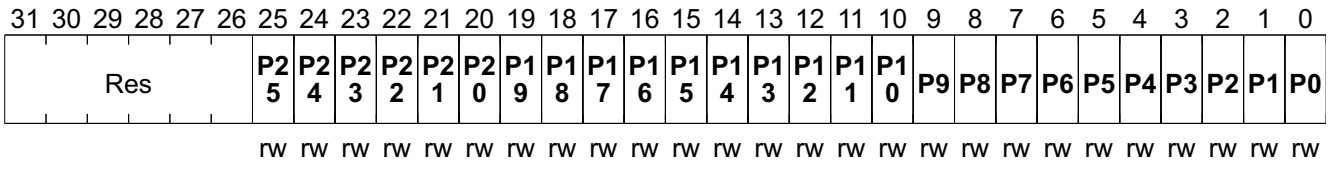
Field	Bits	Type	Description
CI	31:0	ro	**Counter Index** The corresponding counter index by the Bit[7:0] is returned here.

Notes

1. *The Read Counter Control Register and the Read Counter Status Register provide users to read counter if he wants to use fast management clock (fast than 5 MHz).*
2. *Rules:*
   Step 1: Read the Busy bit to check if the read counter module is busy
   Step 2: If the module is free, write the counter index and access bit into the control register
   Step 3: Poll the Busy bit. If Busy = 1'b1, wait. If Busy = 1'b0, read the status register
3. *Example: Users want to read Port 1 Receive Packet Count*
   Step 1: Read Bit[8] to check if the read counter module is busy
   Step 3: Then Port 1 Receive Packet Count will be loaded into the Counter Status Register (Offset: 16_H)
   Step 2: If Bit[8] = 0, then write bit[8] = 1'b1, Bit[7:0] = 8'b1 into the register
   Step 4: Read Counter Status Register (Offset: 16_H) and the content read is the Port 1 Receive Packet Count

Reload MDIO Register

RMDIOR	Offset	Reset Value
Reload MDIO Register	**17_H**	**0000 0000_H**



Field	Bits	Type	Description
P25	25	rw	**Port 25 MDIO Register Reload**
P24	24	rw	**Port 24 MDIO Register Reload**
P23	23	rw	**Port 23 MDIO Register Reload**
P22	22	rw	**Port 22 MDIO Register Reload**
P21	21	rw	**Port 21 MDIO Register Reload**
P20	20	rw	**Port 20 MDIO Register Reload**
P19	19	rw	**Port 19 MDIO Register Reload**
P18	18	rw	**Port 18 MDIO Register Reload**
P17	17	rw	**Port 17 MDIO Register Reload**
P16	16	rw	**Port 16 MDIO Register Reload**
P15	15	rw	**Port 15 MDIO Register Reload**
P14	14	rw	**Port 14 MDIO Register Reload**
P13	13	rw	**Port 13 MDIO Register Reload**
P12	12	rw	**Port 12 MDIO Register Reload**
P11	11	rw	**Port 11 MDIO Register Reload**
P10	10	rw	**Port 10 MDIO Register Reload**
P9	9	rw	**Port 9 MDIO Register Reload**
P8	8	rw	**Port 8 MDIO Register Reload**
P7	7	rw	**Port 7 MDIO Register Reload**
P6	6	rw	**Port 6 MDIO Register Reload**
P5	5	rw	**Port 5 MDIO Register Reload**
P4	4	rw	**Port 4 MDIO Register Reload**
P3	3	rw	**Port 3 MDIO Register Reload**
P2	2	rw	**Port 2 MDIO Register Reload**
P1	1	rw	**Port 1 MDIO Register Reload**
P0	0	rw	**Port 0 MDIO Register Reload** 1_B , Status of Port 0 PHY attached will be reloaded and updated to the switch. After PHY is reloaded, Bit[0] will be cleared.

Spanning Tree Port State 0

STPS0	Offset	Reset Value
Spanning Tree Port State 0	**18_H**	**$0000\ 0000_H$**

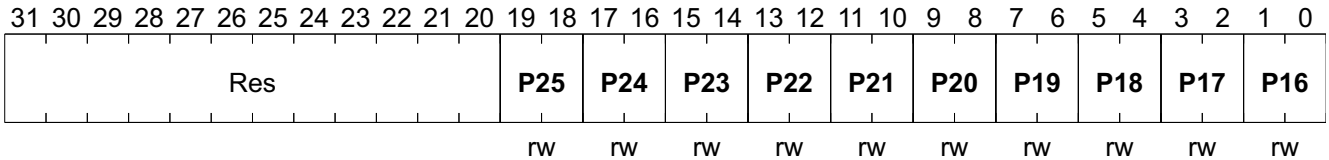
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P15		**P14**		**P13**		**P12**		**P11**		**P10**		**P9**		**P8**		**P7**		**P6**		**P5**		**P4**		**P3**		**P2**		**P1**		**P0**	
rw		rw		rw		rw		rw		rw		rw		rw		rw		rw		rw		rw		rw		rw		rw		rw	

Field	Bits	Type	Description
P15	31:30	rw	**Port 15 Spanning Tree Port Status**
P14	29:28	rw	**Port 14 Spanning Tree Port Status**
P13	27:26	rw	**Port 13 Spanning Tree Port Status**
P12	25:24	rw	**Port 12 Spanning Tree Port Status**
P11	23:22	rw	**Port 11 Spanning Tree Port Status**
P10	21:20	rw	**Port 10 Spanning Tree Port Status**
P9	19:18	rw	**Port 9 Spanning Tree Port Status**
P8	17:16	rw	**Port 8 Spanning Tree Port Status**
P7	15:14	rw	**Port 7 Spanning Tree Port Status**
P6	13:12	rw	**Port 6 Spanning Tree Port Status**
P5	11:10	rw	**Port 5 Spanning Tree Port Status**
P4	9:8	rw	**Port 4 Spanning Tree Port Status**
P3	7:6	rw	**Port 3 Spanning Tree Port Status**
P2	5:4	rw	**Port 2 Spanning Tree Port Status**
P1	3:2	rw	**Port 1 Spanning Tree Port Status**
P0	1:0	rw	**Port 0 Spanning Tree Port Status**

Note: The ADM6926/X supports 4 port status to support Spanning Tree Protocol.00_B = Forwarding State. The port acts as the normal mode.01_B = Disabled State. The port entity will not transmit and receive any packets. Learning is disabled in this state.10_B = Learning State. The port entity will only transmit and receive management packets. All other packets are discarded. Learning is enabled for all good frames.11_B = Blocking-not-Listening. Only the management packets defined by the ADM6926/X will be received and transmitted.
All other packets are discarded by the port entity. Learning is disabled in this state.

Spanning Tree Port State 1

STPS1	Offset	Reset Value
Spanning Tree Port State 1	**19_H**	**$0000\ 0000_H$**

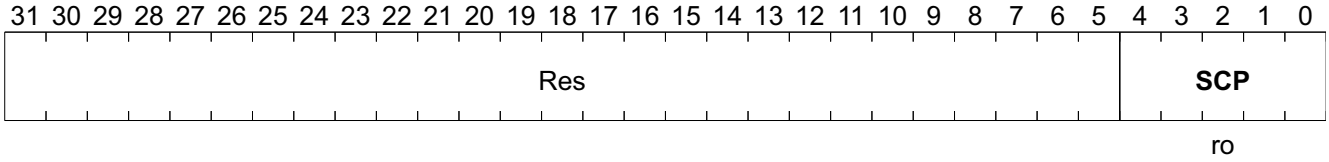


Field	Bits	Type	Description
P25	19:18	rw	**Port 25 Spanning Tree Port Status**
P24	17:16	rw	**Port 24 Spanning Tree Port Status**
P23	15:14	rw	**Port 23 Spanning Tree Port Status**
P22	13:12	rw	**Port 22 Spanning Tree Port Status**

Field	Bits	Type	Description
P21	11:10	rw	**Port 21 Spanning Tree Port Status**
P20	9:8	rw	**Port 20 Spanning Tree Port Status**
P19	7:6	rw	**Port 19 Spanning Tree Port Status**
P18	5:4	rw	**Port 18 Spanning Tree Port Status**
P17	3:2	rw	**Port 17 Spanning Tree Port Status**
P16	1:0	rw	**Port 16 Spanning Tree Port Status**

Source Port Register

SCPR	Offset	Reset Value
Source Port Register	**$1A_H$**	**0000_0000_H**

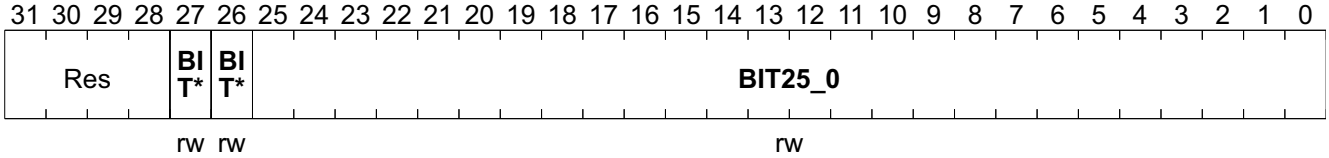


Field	Bits	Type	Description
SCP	4:0	ro	**The Source Port** The CPU can read this register to get the source port when he receives a packet.

Note: The value will be correct after the SA is transmitted.

Transmit Port Register

TRPR	Offset	Reset Value
Transmit Port Register	**$1B_H$**	**$0000\ 0000_H$**



Field	Bits	Type	Description
BIT27	27	rw	**Bit 27** 0_B , The command is not valid. 1_B , The command is valid.

Field	Bits	Type	Description
BIT26	26	rw	**Bit 26** The destination ports is more than 1
BIT25_0	25:0	rw	**Bit 25_0** The destination ports the CPU wants to forward.

Note: The value should be written before CPU transmits a packet.

Counter Register

Offset **0100_H ~ $019B_H$**

Table 30 Counter Register: Offset 0100_H ~ 0167_H

Offset Hex	Index	Description	Offset Hex	Index	Description
The Receive Count					
0100	0	Port 0 Receive Packet Count	011A	1A	Port 0 Receive Packet Length Count
0101	1	Port 1 Receive Packet Count	011B	1B	Port 1 Receive Packet Length Count
0102	2	Port 2 Receive Packet Count	011C	1C	Port 2 Receive Packet Length Count
0103	3	Port 3 Receive Packet Count	011D	1D	Port 3 Receive Packet Length Count
0104	4	Port 4 Receive Packet Count	011E	1E	Port 4 Receive Packet Length Count
0105	5	Port 5 Receive Packet Count	011F	1F	Port 5 Receive Packet Length Count
0106	6	Port 6 Receive Packet Count	0120	20	Port 6 Receive Packet Length Count
0107	7	Port 7 Receive Packet Count	0121	21	Port 7 Receive Packet Length Count
0108	8	Port 8 Receive Packet Count	0122	22	Port 8 Receive Packet Length Count
0109	9	Port 9 Receive Packet Count	0123	23	Port 9 Receive Packet Length Count
010A	A	Port 10 Receive Packet Count	0124	24	Port 10 Receive Packet Length Count
010B	B	Port 11 Receive Packet Count	0125	25	Port 11 Receive Packet Length Count
010C	C	Port 12 Receive Packet Count	0126	26	Port 12 Receive Packet Length Count
010D	D	Port 13 Receive Packet Count	0127	27	Port 13 Receive Packet Length Count
010E	E	Port 14 Receive Packet Count	0128	28	Port 14 Receive Packet Length Count

Table 30 Counter Register: Offset 0100_H ~ 0167_H (cont'd)

Offset Hex	Index	Description	Offset Hex	Index	Description
010F	F	Port 15 Receive Packet Count	0129	29	Port 15 Receive Packet Length Count
0110	10	Port 16 Receive Packet Count	012A	2A	Port 16 Receive Packet Length Count
0111	11	Port 17 Receive Packet Count	012B	2B	Port 17 Receive Packet Length Count
0112	12	Port 18 Receive Packet Count	012C	2C	Port 18 Receive Packet Length Count
0113	13	Port 19 Receive Packet Count	012D	2D	Port 19 Receive Packet Length Count
0114	14	Port 20 Receive Packet Count	012E	2E	Port 20 Receive Packet Length Count
0115	15	Port 21 Receive Packet Count	012F	2F	Port 21 Receive Packet Length Count
0116	16	Port 22 Receive Packet Count	0130	30	Port 22 Receive Packet Length Count
0117	17	Port 23 Receive Packet Count	0131	31	Port 23 Receive Packet Length Count
0118	18	Port 24 Receive Packet Count	0132	32	Port 24 Receive Packet Length Count
0119	19	Port 25 Receive Packet Count	0133	33	Port 25 Receive Packet Length Count
The Transmit Count					
0134	34	Port 0 Transmit Packet Count	014E	4E	Port 0 Transmit Packet Length Count
0135	35	Port 1 Transmit Packet Count	014F	4F	Port 1 Transmit Packet Length Count
0136	36	Port 2 Transmit Packet Count	0150	50	Port 2 Transmit Packet Length Count
0137	37	Port 3 Transmit Packet Count	0151	51	Port 3 Transmit Packet Length Count
0138	38	Port 4 Transmit Packet Count	0152	52	Port 4 Transmit Packet Length Count
0139	39	Port 5 Transmit Packet Count	0153	53	Port 5 Transmit Packet Length Count
013A	3A	Port 6 Transmit Packet Count	0154	54	Port 6 Transmit Packet Length Count
013B	3B	Port 7 Transmit Packet Count	0155	55	Port 7 Transmit Packet Length Count
013C	3C	Port 8 Transmit Packet Count	0156	56	Port 8 Transmit Packet Length Count
013D	3D	Port 9 Transmit Packet Count	0157	57	Port 9 Transmit Packet Length Count

Table 30 Counter Register: Offset 0100_H ~ 0167_H (cont'd)

Offset Hex	Index	Description	Offset Hex	Index	Description
013E	3E	Port 10 Transmit Packet Count	0158	58	Port 10 Transmit Packet Length Count
013F	3F	Port 11 Transmit Packet Count	0159	59	Port 11 Transmit Packet Length Count
0140	40	Port 12 Transmit Packet Count	015A	5A	Port 12 Transmit Packet Length Count
0141	41	Port 13 Transmit Packet Count	015B	5B	Port 13 Transmit Packet Length Count
0142	42	Port 14 Transmit Packet Count	015C	5C	Port 14 Transmit Packet Length Count
0143	43	Port 15 Transmit Packet Count	015D	5D	Port 15 Transmit Packet Length Count
0144	44	Port 16 Transmit Packet Count	015E	5E	Port 16 Transmit Packet Length Count
0145	45	Port 17 Transmit Packet Count	015F	5F	Port 17 Transmit Packet Length Count
0146	46	Port 18 Transmit Packet Count	0160	60	Port 18 Transmit Packet Length Count
0147	47	Port 19 Transmit Packet Count	0161	61	Port 19 Transmit Packet Length Count
0148	48	Port 20 Transmit Packet Count	0162	62	Port 20 Transmit Packet Length Count
0149	49	Port 21 Transmit Packet Count	0163	63	Port 21 Transmit Packet Length Count
014A	4A	Port 22 Transmit Packet Count	0164	64	Port 22 Transmit Packet Length Count
014B	4B	Port 23 Transmit Packet Count	0165	65	Port 23 Transmit Packet Length Count
014C	4C	Port 24 Transmit Packet Count	0166	66	Port 24 Transmit Packet Length Count
014D	4D	Port 25 Transmit Packet Count	0167	67	Port 25 Transmit Packet Length Count
Error and Collision Count					
0168	68	Port 0 Receive Error Count	0182	82	Port 0 Collision Count
0169	69	Port 1 Receive Error Count	0183	83	Port 1 Collision Count
016A	6A	Port 2 Receive Error Count	0184	84	Port 2 Collision Count
016B	6B	Port 3 Receive Error Count	0185	85	Port 3 Collision Count
016C	6C	Port 4 Receive Error Count	0186	86	Port 4 Collision Count
016D	6D	Port 5 Receive Error Count	0187	87	Port 5 Collision Count
016E	6E	Port 6 Receive Error Count	0188	88	Port 6 Collision Count
016F	6F	Port 7 Receive Error Count	0189	89	Port 7 Collision Count
0170	70	Port 8 Receive Error Count	018A	8A	Port 8 Collision Count
0171	71	Port 9 Receive Error Count	018B	8B	Port 9 Collision Count

Table 30 Counter Register: Offset 0100_H ~ 0167_H (cont'd)

Offset Hex	Index	Description	Offset Hex	Index	Description
0172	72	Port 10 Receive Error Count	018C	8C	Port 10 Collision Count
0173	73	Port 11 Receive Error Count	018D	8D	Port 11 Collision Count
0174	74	Port 12 Receive Error Count	018E	8E	Port 12 Collision Count
0175	75	Port 13 Receive Error Count	018F	8F	Port 13 Collision Count
0176	76	Port 14 Receive Error Count	0190	90	Port 14 Collision Count
0177	77	Port 15 Receive Error Count	0191	91	Port 15 Collision Count
0178	78	Port 16 Receive Error Count	0192	92	Port 16 Collision Count
0179	79	Port 17 Receive Error Count	0193	93	Port 17 Collision Count
017A	7A	Port 18 Receive Error Count	0194	93	Port 18 Collision Count
017B	7B	Port 19 Receive Error Count	0195	95	Port 19 Collision Count
017C	7C	Port 20 Receive Error Count	0196	96	Port 20 Collision Count
017D	7D	Port 21 Receive Error Count	0197	97	Port 21 Collision Count
017E	7E	Port 22 Receive Error Count	0198	98	Port 22 Collision Count
017F	7F	Port 23 Receive Error Count	0199	99	Port 23 Collision Count
0180	80	Port 24 Receive Error Count	019A	9A	Port 24 Collision Count
0181	81	Port 25 Receive Error Count	019B	9B	Port 25 Collision Count

3.3.2 Address Table Control and Status Registers

- Address Table Control Register 0 (Offset: 5_H)
- Address Table Control Register 1 (Offset: 6_H)
- Address Table Control Register 2 (Offset:7_H)
- Address Table Status Register 0 (Offset: 8_H)
- Address Table Status Register 1 (Offset: 9_H)
- Address Table Status Register 2 (Offset: A_H)

The ADM6926/X provides custom commands to access the address table as well as the multicast output port map table. Six registers are used and they mean differently when different tables are accessed.

3.3.2.1 Control and Status Register for the Address Table

The Control and Status Register Description

Table 31 Control Register Description

Command Field	Entry State	Control Field	Output Port/ Multicast Index	Forwarding Group	MAC Address
Control_2[2:0]	Control_1[31:30]	Control_1[29:26]	Control_1[25:21]	Control_1[20:16]	{Control_1[15:0], Control_0[31:0]}

Table 32 Field Description in the Control Register

Field	Description		
MAC Address[47:0]	This field is 48-bit layer-2 address. The address could be the unicast address or the multicast address.		
Forwarding Group[4:0]	This field describes the Learning Group the address belongs to.		
Output Port[4:0]/Multicast Index[4:0]	This field has two means. One is described as the output port and the other is described as the multicast index.		
Entry State[0]	The Static Bit. When this bit is set to a one, then the address entry will not be aged forever. This bit could be changed only through the CUP's help.		
Entry State[1]	This bit is used to distinguish the output port/ multicast index field. When a match (the same MAC address and the same forwarding group in the address table) is found, the value in the output port field is returned as the output port, and may be modified by the forwarding group before the packet is transferred to the output queue. When a match (the same MAC address and the same forwarding group in the address table) is found, the multicast output port map entry addressed by the multicast index is returned as the output port map, and may be modified by the forwarding group before the packet is transferred to the output queue.		
Command Field[2:0]/ Control Field[3:0]	The command and control fields are combined to provide different operations. Before the operation is initiated, users should confirm if the search engine is available. See the busy bit in the status register.		
	Command Field	Control Field	Operation
	000	0111	Create a new address
	000	1111	Overwrite an existed address
	001	1111	Erase an existed address
	010	0000	Search an empty address
	010	1001	Search by the port in the Output Port field
	010	1010	Search by the forwarding group specified in the Forwarding Group field
	010	1100	Search by the address specified in the MAC Address field
	010	1110	Search by the address and forwarding group
	010	1101	Search by the address and output port
	010	1011	Search by the forwarding group and the output port
	010	1111	Search by the address, the forwarding group and the output port
	011	0100	Initial to location by the address field
	011	0000	Initial to the first address

Table 33 Status Register Description

Busy	Command Result	Bad State	Entry State	Occupy	Output Port/ Multicast Index	Forwarding Group	MAC Address
Status_2[3]	Status_2 [2:0]	Status_1 [29]	Status_1 [28:27]	Status_1 [26]	Status_1 [25:21]	Status_1 [20:16]	{Status_1 [15:0], Status_0 [31:0]}

Table 34 Field Description in the Status Register

Field	Description
MAC Address[47:0]	After the search operation is successful, the switch will return the MAC address in this field. If the search fails, this field doesn't mean anything.
Forwarding Group[4:0]	After the search operation is successful, the switch will return the Forwarding Group in this. If the search fails, this field doesn't mean anything.
Output Port[4:0]/ Multicast Index[4:0]	After the search operation is successful, the switch will return output port / multicast index in this field. The users could use the entry_state[1] returned to distinguish if the entry should point to the multicast output port map table.
Occupy	After the search is successful, the switch will return the value indicating if the entry existed. 0_B , The searched entry doesn't exist. 1_B , The searched entry exists.
Entry State[0]	After the search is successful, the switch will return the value in this field indicating if value is static. 0_B , The searched entry is not static and will be aged. 1_B , The searched entry is static.
Entry State[1]	After the search is successful, the switch will return the value in this field indicating if the entry points to the multicast output port map table. 0_B , The entry doesn't point to the multicast output port map table. 1_B , The entry points to the multicast output port map table.
Bad State	After the search is successful, the switch will return the value indicating if the entry is bad. 0_B , The entry is not bad and will be used for data storage. 1_B , The entry is bad and isn't used for data storage.
Command Result[2:0]	This field indicates the access result. 000_B , Command OK. 001_B , All Entry Used. This result happens only for the create operation. ADM6926/X uses the 4-way address lookup engine so it allows 4 different addresses stored at each hash location. If these 4 entries are all static, then CPU will not successfully create 5th different address hashed to the same location and 001 will be returned. The only way to create 5th different address is to remove one of early addresses. 010_B , Entry Not Found. 011_B , Try Next Entry. 101_B , Command Error.
Busy	This bit indicates if the table engine for access is available. 0_B , The engine is available. 1_B , The engine is busy and it will not access the command from the CPU.

Rules to Access the Address Table

1. Check the Busy Bit in the status register to see if the access engine is available. If the engine is busy, wait until the engine is free. If the engine is available, go to the following step.
2. Write the MAC address[31:0] into the control register 0.
3. Write the MAC address[47:32], Forwarding Group, Output Port/Multicast Index, Control Field and the Entry State into the control register 1.
4. Write the Command into the control register 2 to define the operation.
5. Wait for the engine to complete (Check the Busy Bit).
6. Read the desired result returned in the status register.

Note: Before the "Search command", the CPU should execute the "Initial command" to initial the search pointer. The search engine could search the aim from the top to the bottom. The search engine has an ability to automatically move the pointer to the associated location (The result will be returned). Because more than one entry may match the searching condition (by port, by address, etc.) at the same time, the CPU should continue to restart the search engine until the Command Result = Entry Not is found to confirm that no other matching entries exist.

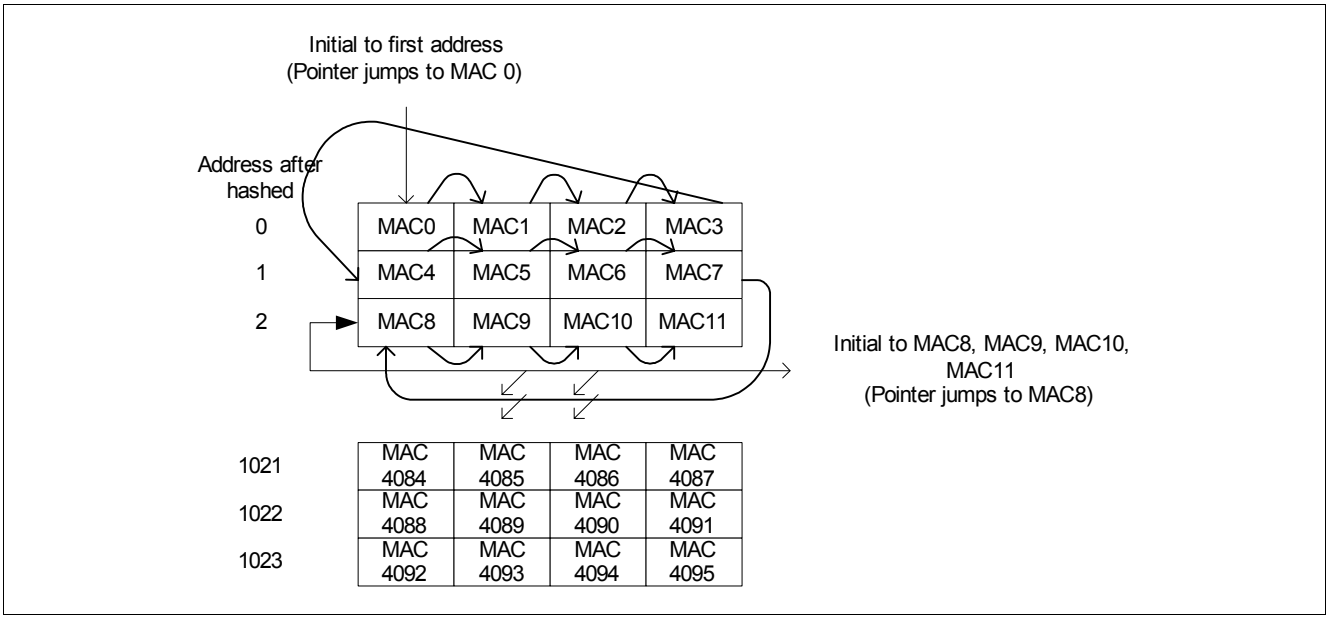


Figure 11 The Search Pointer

Example

Table 35 Example

Example	Step
The user needs ADM6926/X to forward the specified unicast packet (DA = 48'h0012_3456_789a and Forwarding Group = 2) to port 3 forever.	Step 1: Check the Busy bit. If Busy = 0_B, go to the step 2. If Busy = 1_B, wait. Step 2: Write 3456_789A$_H$ into control register 0. Step 3: Write 5C62_0012$_H$ into the control register 1. Step 4: Write 0000_0000$_H$ into the control register 2 to start the "Create" operation. Step 5: Read the status register 2 to check the busy bit. If Busy = 0_B, check the Command Result to see if the create operation is successful. If Busy = 1_B, wait for completion.
The user needs the ADM6926/X to forward the specified multicast packet (DA = 48'h0123_4567_89ab and Forwarding Group = 3) to port 5 only. This address could be aged.	Step 1: Check the Busy bit. If Busy = 0_B, go to the step 2. If Busy = 1_B, wait. Step 2: Write 4567_89AB$_H$ into control register 0. Step 3: Write 1CA3_0123$_H$ into the control register 1. Step 4: Write 0000_0000$_H$ into the control register 2 to start the "Create" operation. Step 5: Read the status register 2 to check the busy bit. If Busy = 0_B, check the Command Result to see if the create operation is successful. If Busy = 1_B, wait for completion.
The user wants to know how many stations attached to port 4.	Step 1: Check the Busy bit. If Busy = 0_B, go to the step 2. If Busy = 1_B, wait. Step 2: Write 0000_0000$_H$ into control register 1. Step 3: Write 0000_0003$_H$ into control register 2 to start the "Initial to the first address" operation. Step 4: Read the status register 2 to check the busy bit. If Busy = 0_B, check the Command Result to see if the initial operation is successful. If Busy = 1_B, wait for completion. Step 5: Write 2480_0000$_H$ into control register 1. Step 6: Write 0000_0002$_H$ into control register 2 to start the "Search by port" operation. Step 7: Read the status register 2 to check the busy bit. If Busy = 0_B, check the Command Result to see if the search operation is successful (the Mac address attached to port 4 could be derived from the MAC address in the status register). If Busy = 1_B, wait for completion. Step 8: If Command Result = "Command OK", it means some other MAC addresses attached to port 4 may exist. We should restart the "Search by port" command again to let the search engine to look another addresses. Step 9: If the Command Result = "Entry Not Found", it means no other addresses attached to port 4 exist.

3.3.2.2 Control and Status Register for the Multicast Output Port Map Table

The Control and Status Register Description

Table 36 Control Register Description

Command Field	Multicast Index	Output Port Map
Control_2[2:0]	Control_0[30:26]	Control_0[25:0]

Table 37 Field Description in the Control Register

Field	Description
Output Port Map	This field describes the output ports associated with the multicast index.Bit [0] is for port 0, Bit[1] is for port 1, … and Bit[25] for port 25.
Multicast Index	Refer to **Figure 12**
Command Field	100_B , Create an entry in the output port map table (indexed by the Multicast Index). 101_B , Search an entry in the output port map table (indexed by the Multicast Index).

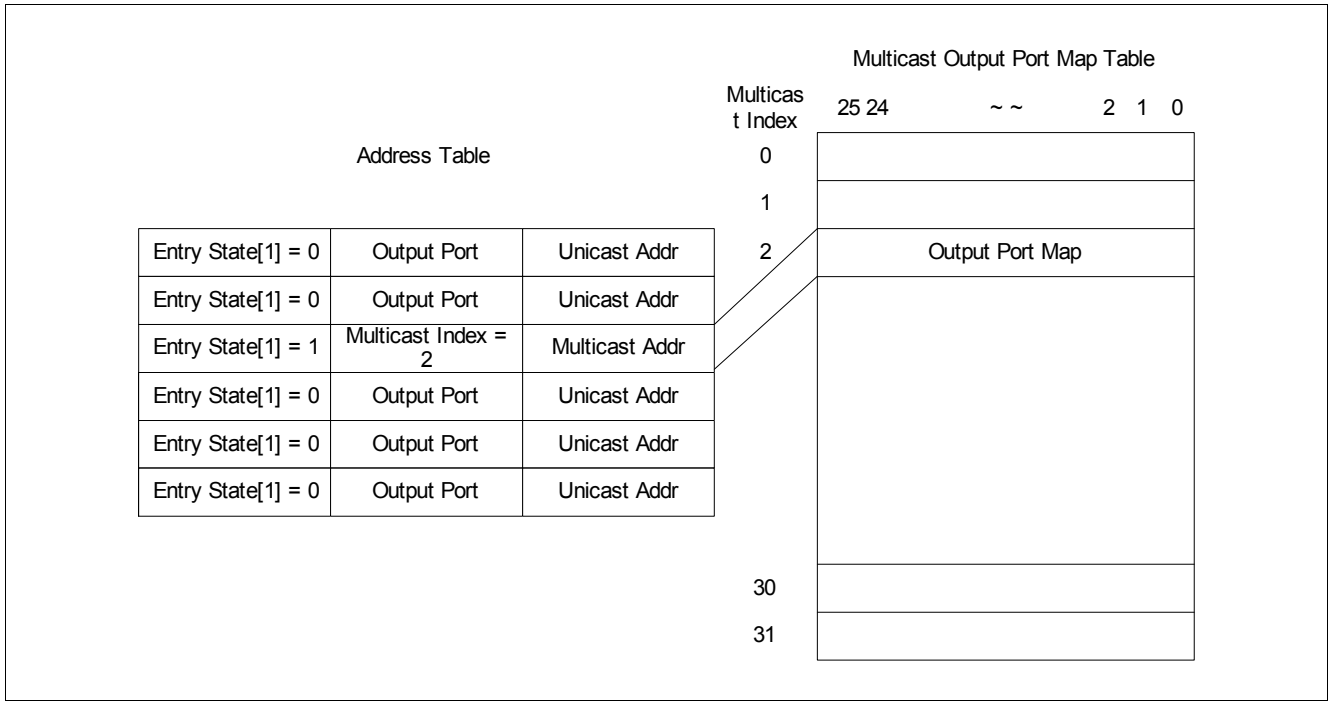


Figure 12 Address Table Mapping to Output Port MAP

Table 38 Status Register Description

Busy	Command Result	Output Port Map
Status_2[3]	Status_2[2:0]	Status_0[25:0]

Table 39 Field Description in the Status Register

Field	Description
Output Port Map	The content associated with the multicast index will be here after searching.
Command Result	000_B = Command OK
Busy	This bit indicates if the output port map engine is available. 0_B , The engine is available. 1_B , The engine is busy and it will not access the command from the CPU.

Rules to Access the Multicast Output Port Map Table

1. Check the Busy Bit to see if the access engine is available. If the engine is busy, wait until the engine is free. If the engine is available, go to the following step.
2. Write output port map and the multicast index into the control register 0.
3. Write the command into the control register 2.

4. Read the Busy Bit. If Busy = 1_B, wait. If Busy = 0_B, the operation completes.

Example

Table 40 Example

Example	Step
The user needs the ADM6926/X to forward the specified multicast packet (DA = $0123\_4567\_89AB_H$ and Forwarding Group = 3) to port 1, port2 and port 25. This address could be aged. We assume the CPU wants to write output port map into index 1.	Step 1: Check the Busy bit. If Busy = 0_B, go to the step 2. If Busy = 1_B, wait. Step 2: Write 0060_0006_H into control register 0. Step 3: Write 0000_0004_H into control register 2 start the “Write” command. Step 4: Check the Busy bit. If Busy = 1_B, wait. If Busy = 0_B, go to the next step. Step 5: Write 4567_89AB_H into control register 0. Step 6: Write $9C23\_0123_H$ into the control register 1. Step 7: Write 0000_0000_H into the control register 2 to start the “Create” operation. Step 8: Read the status register 2 to check the busy bit. If Busy = 0_B, check the Command Result to see if the create operation is successful. If Busy = 1_B, wait for completion.

4 Electrical Specifications

4.1 DC Characteristics

Table 41 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
3.3 V Power Supply	V_{CCO}	3.0	–	3.6	V	–
1.8 V Power Supply	V_{CCIK}	1.71	–	1.89	V	–
Input Voltage	V_{IN}	-0.3	–	$V_{CC\ 33}$ + 0.3	V	–
Output Voltage	V_{out}	-0.3	–	$V_{CC\ 33}$ + 0.3	V	–
Storage Temperature	T_{STG}	-55	–	155	°C	–
Power Dissipation	P_D	–	–	1.0	W	–
ESD Rating	ESD	–	–	3000	V	–

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

Table 42 Recommended Operating Conditions

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Power Supply	V_{CC}	3.135	3.3	3.465	V	–
Input Voltage	V_{IN}	0	–	V_{CC}	V	–
Junction Operating Temperature	T_j	0	25	115	°C	–

Table 43 DC Electrical Characteristics for 3.3 V Operation[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input Low Voltage	V_{IL}	–	–	0.8	V	TTL
Input High Voltage	V_{IH}	2.0	–	–	V	TTL
Output Low Voltage	V_{OL}	–	–	0.4	V	TTL
Output High Voltage	V_{OH}	2.3	–	–	V	TTL
Input Pull-up/down Resistance	R_I	–	50	–	KΩ	V_{IL} = 0 V or V_{IH} = V_{CC}

1) Under V_{CC} = 3.0 V ~ 3.6 V, T_j = 0 °C ~ 115 °C

4.2 AC Characteristics

4.2.1 XI/OSCI (Crystal/Oscillator) Timing

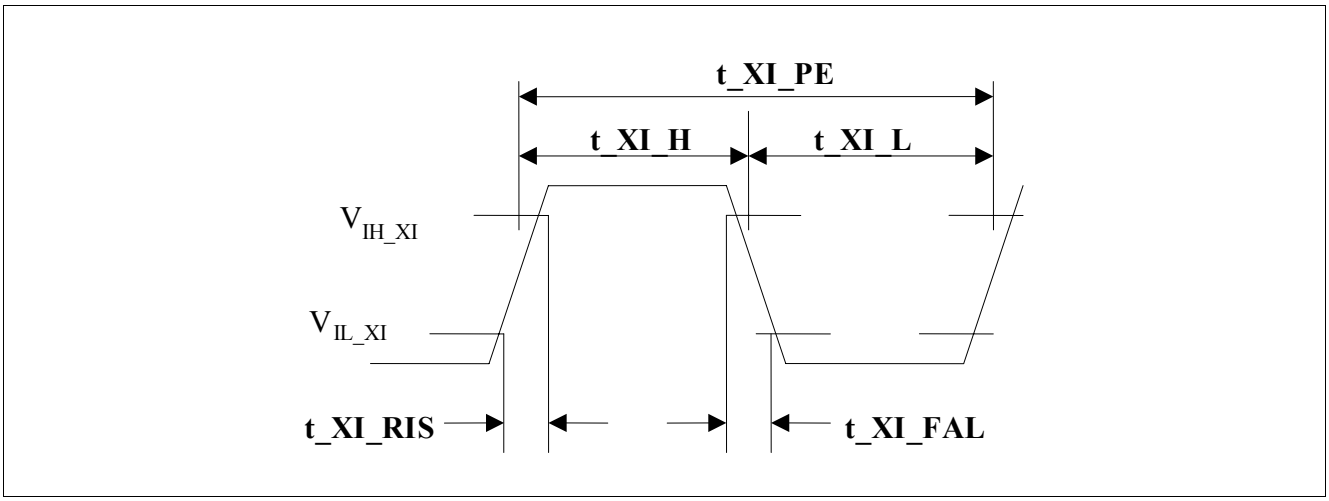


Figure 13 Crystal/Oscillator Timing

Table 44 Crystal/Oscillator Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
XI/OSCI Clock Period	t_{XI_PER}	20.0 - 50ppm	20.0	20.0 + 50ppm	ns	–
XI/OSCI Clock High	t_{XI_HI}	8	10.0	–	ns	–
XI/OSCI Clock Low	t_{XI_LO}	8	10.0	–	ns	–
XI/OSCI Clock Rise Time, V_{IL} (max) to V_{IH} (min.)	t_{XI_RISE}	–	–	2	ns	–
XI/OSCI Clock Fall Time, V_{IH} (min.) to V_{IL} (max)	t_{XI_FALL}	–	–	2	ns	–

4.2.2 Power On Reset

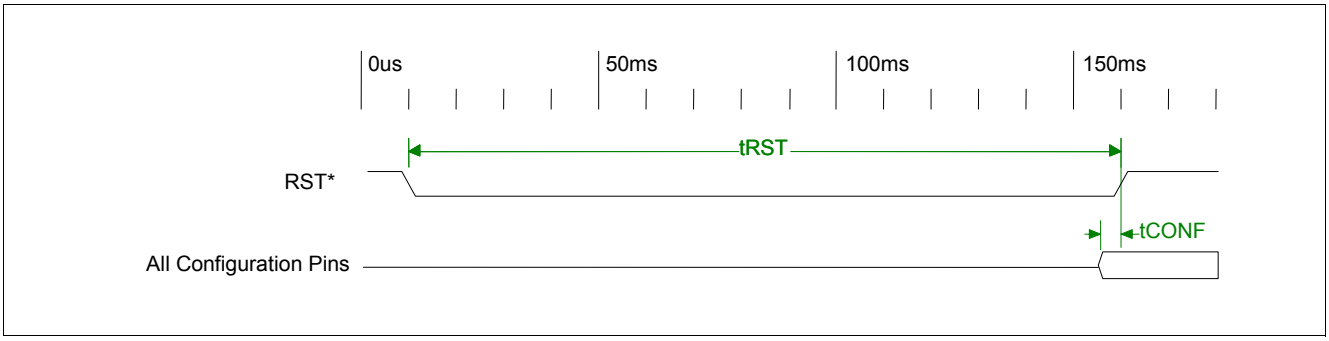


Figure 14 Power on Reset Timing

Table 45 Power on Reset Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
RST Low Period	t_{RST}	150	–	–	ms	–
Start of Configuration Pins	t_{CONF}	100	–	–	ns	–

4.2.3 EEPROM Interface Timing

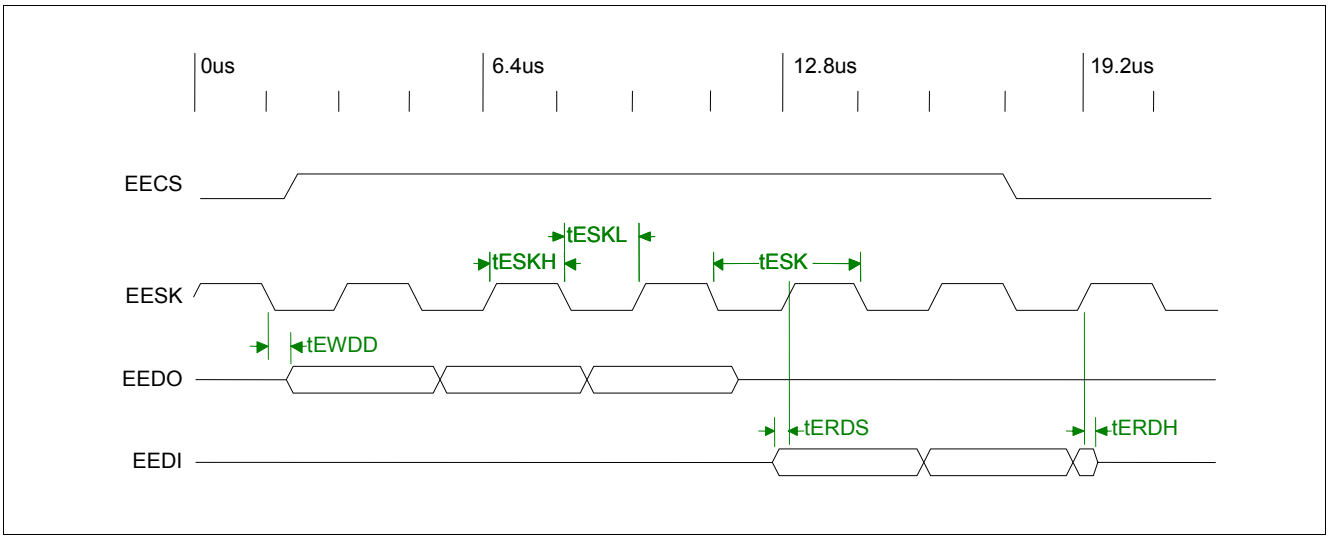


Figure 15 EEPROM Interface Timing

Table 46 EEPROM Interface Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
EESK Period	t_{ESK}	–	3.2	–	µs	–
EESK Low Period	t_{ESKL}	–	1.6	–	µs	–
EESK High Period	t_{ESKH}	–	1.6	–	µs	–
EEDI to EESK Rising Setup Time	t_{ERDS}	10	–	–	ns	–
EEDI to EESK Rising Hold Time	t_{ERDH}	10	–	–	ns	–
EESK Falling to EEDO Output Delay Time	t_{EWDD}	–	–	20	ns	–

4.2.4 10Base-TX MII Output Timing

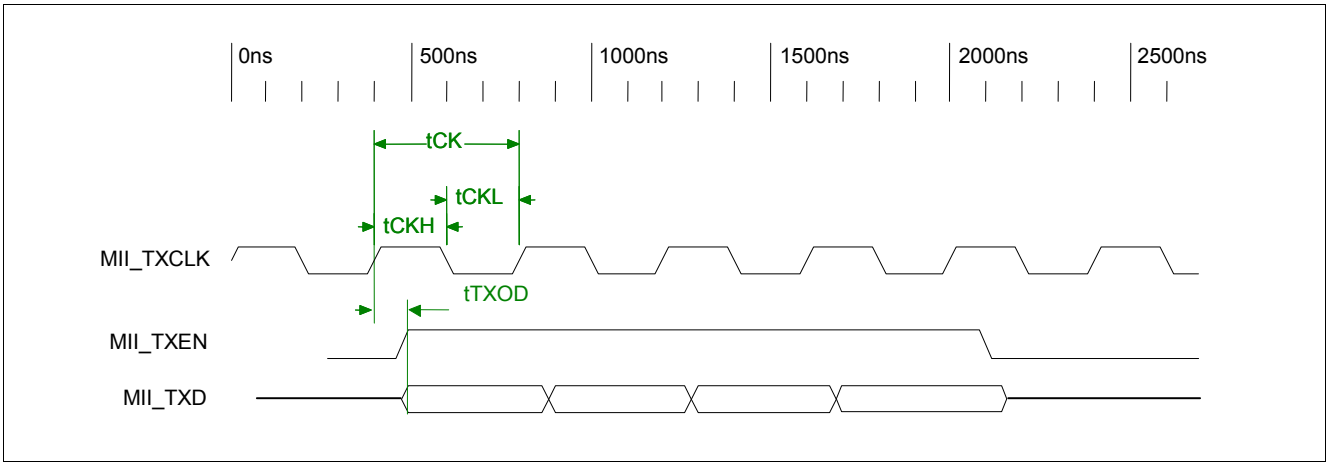


Figure 16 10Base-TX MII Output Timing

Table 47 10Base-TX MII Output Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
MII_TXCLK Period	t_{CK}	–	400	–	ns	–
MII_TXCLK Low Period	t_{CKL}	160	–	240	ns	–
MII_TXCLK High Period	t_{CKH}	160	–	240	ns	–
MII_TXD, MII_TXEN to MII_TXCLK Rising Output Delay	t_{TXOD}	10	–	20	ns	–

4.2.5 10Base-TX MII Input Timing

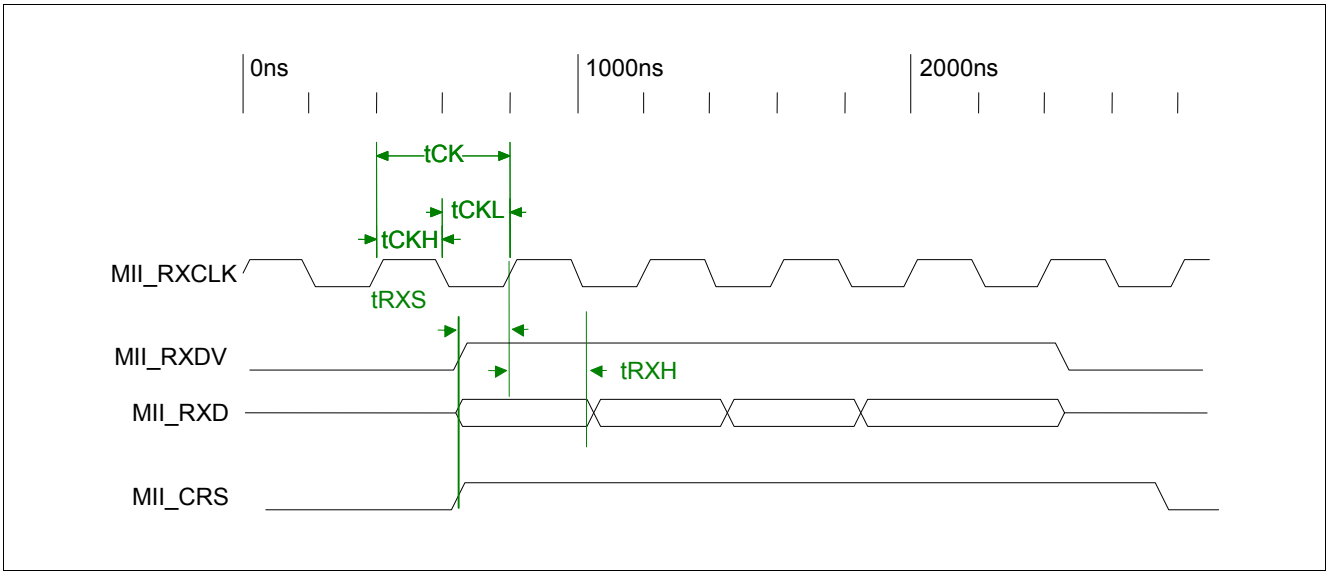


Figure 17 10Base-TX MII Input Timing

Table 48 10Base-TX MII Input Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
MII_RXCLK Period	t_{CK}	–	400	–	ns	–
MII_RXCLK Low Period	t_{CKL}	160	–	240	ns	–
MII_RXCLK High Period	t_{CKH}	160	–	240	ns	–
MII_CRS, MII_RXDV and MII_RXD to MII_RXCLK rising setup	t_{RXS}	10	–	–	ns	–
MII_CRS, MII_RXDV and MII_RXD to MII_RXCLK rising hold	t_{RXH}	10	–	–	ns	–

4.2.6 100Base-TX MII Output Timing

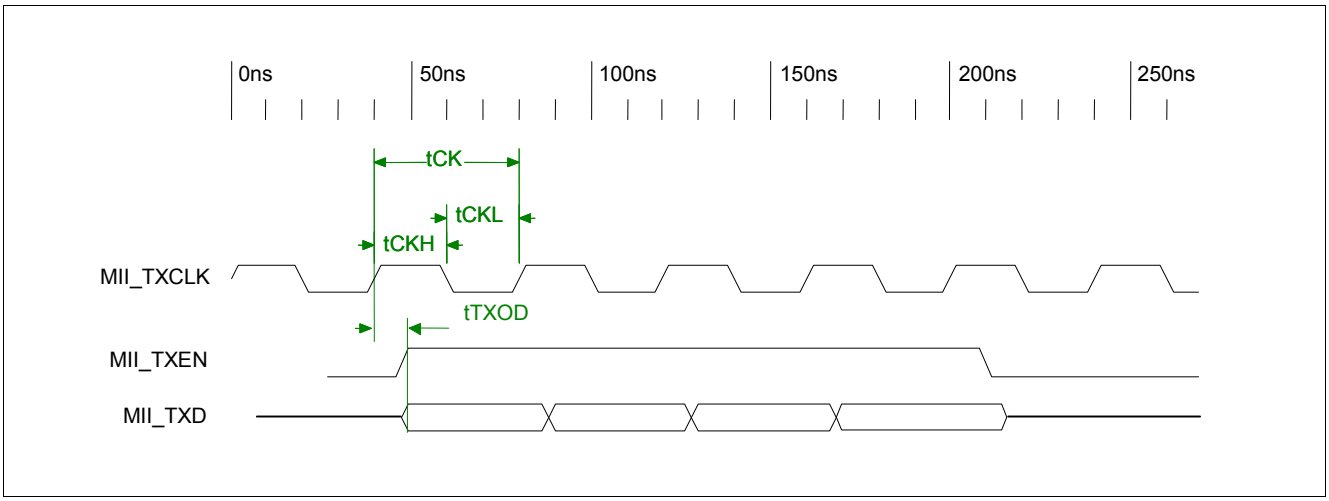


Figure 18 100Base-TX MII Output Timing

Table 49 100Base-TX MII Output Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
MII_TXCLK Period	t_{CK}	–	40	–	ns	–
MII_TXCLK Low Period	t_{CKL}	16	–	24	ns	–
MII_TXCLK High Period	t_{CKH}	16	–	24	ns	–
MII_TXD, MII_TXEN to MII_TXCLK Rising Out put Delay	t_{TXOD}	10	–	20	ns	–

4.2.7 100Base-TX MII Input Timing

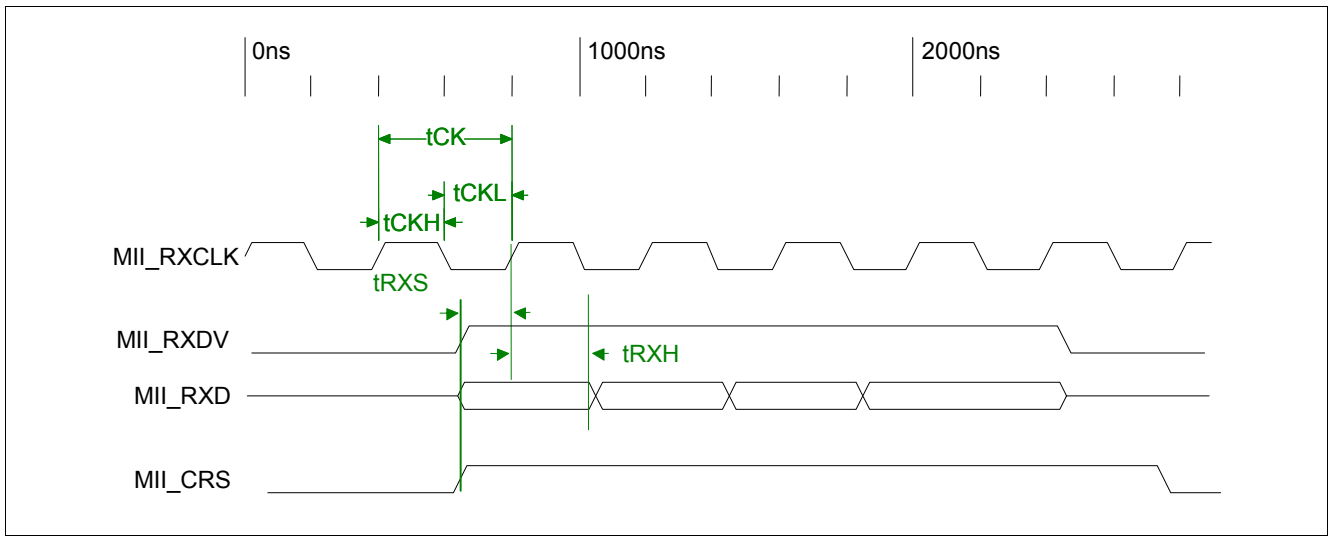


Figure 19 100Base-TX MII Input Timing

Table 50 100Base-TX MII Input Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
MII_RXCLK Period	t_{CK}	–	40	–	ns	–
MII_RXCLK Low Period	t_{CKL}	16	–	24	ns	–
MII_RXCLK High Period	t_{CKH}	16	–	24	ns	–
MII_CRS, MII_RXDV and MII_RXD to MII_RXCLK rising setup	t_{RXS}	10	–	–	ns	–
MII_CRS, MII_RXDV and MII_RXD to MII_RXCLK rising hold	t_{RXH}	10	–	–	ns	–

4.2.8 Reduced MII Timing

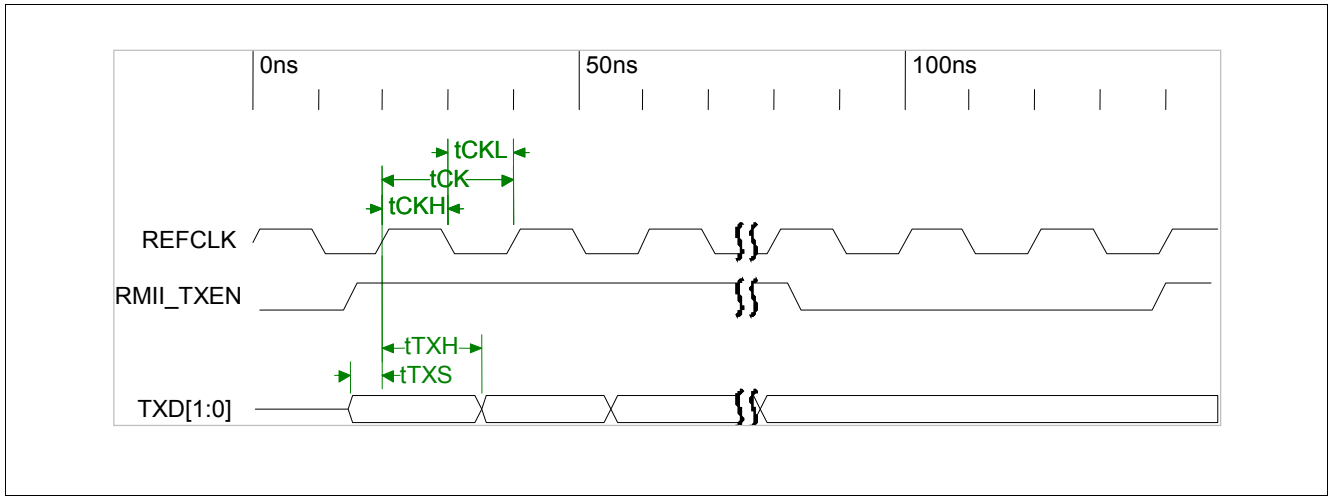


Figure 20 Reduced MII Timing (1 of 2)

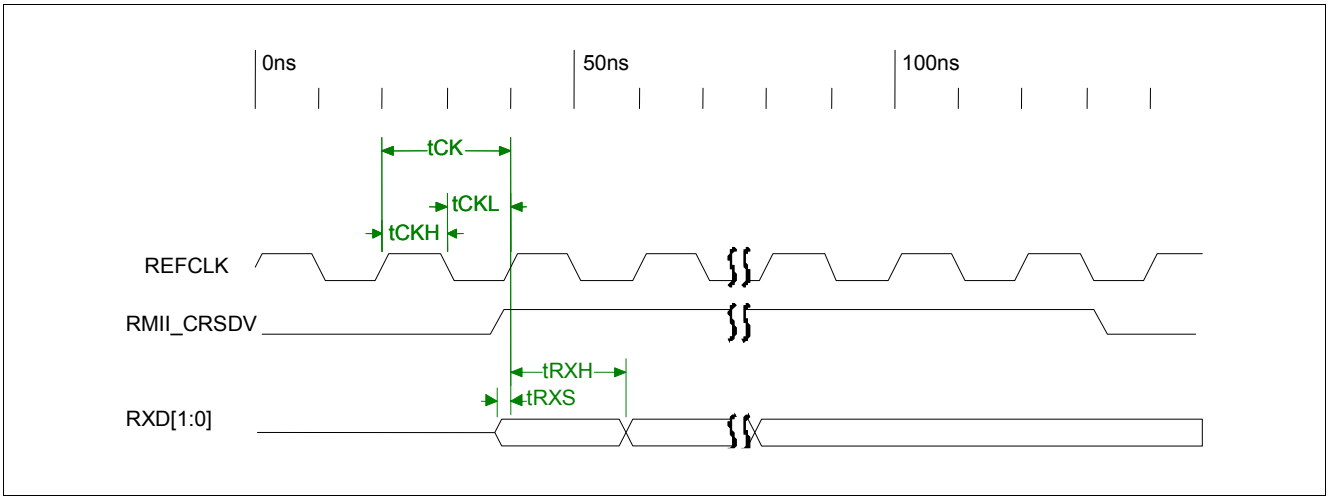


Figure 21 Reduced MII Timing (2 of 2)

Table 51 Reduced MII Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
RMII_REFCLK Period	t_{CK}	–	20	–	ns	–
RMII_REFCLK Low Period	t_{CKL}	–	10	–	ns	–
RMII_REFCLK High Period	t_{CKH}	–	10	–	ns	–
TXEN, TXD to REFCLK rising setup time	t_{TXS}	4	–	–	ns	–
TXEN, TXD to REFCLK rising hold time	t_{TXH}	2	–	–	ns	–
CSRDV, RXD to REFCLK rising setup time	t_{RXS}	4	–	–	ns	–
CRSDV, RXD to REFCLK rising hold time	t_{RXH}	2	–	–	ns	–

4.2.9 SS_SMII Transmit Timing

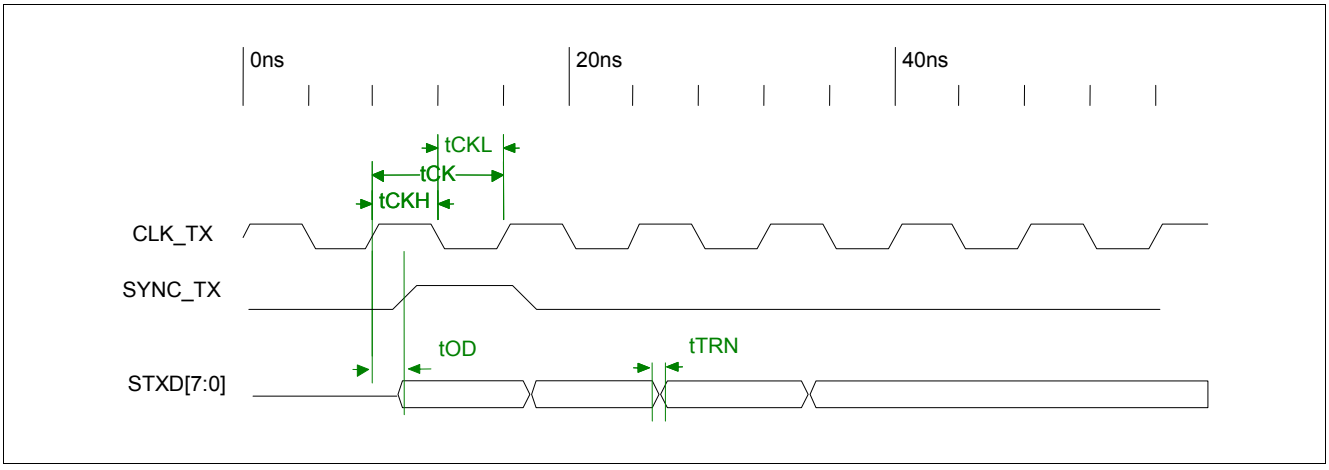


Figure 22 SS_SMII Transmit Timing

Table 52 SS_SMII Transmit Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SS_SMII Output Clock Period	t_{CK}	–	8	–	ns	–
SS_SMII Output Clock Low Period	t_{CKL}	–	4	–	ns	–
R SS_SMII Output Clock High Period	t_{CKH}	–	4	–	ns	–
Txdata/TxSync output delay to CLK_TX	t_{OD}	2	–	5	ns	–
Txdata/RxSync Rise/Fall Time	t_{TRN}	–	1	–	ns	–

4.2.10 SS_SMII Receive Timing

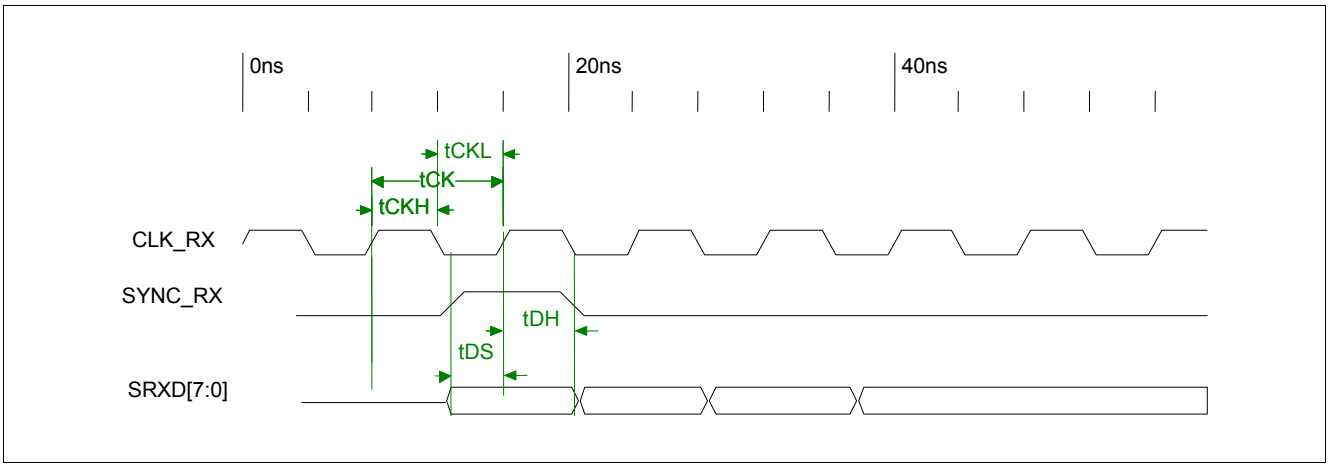


Figure 23 SS_SMII Receive Timing

Table 53 SS_SMII Receive Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SS_SMII CLK_RX Clock Period	t_{CK}	–	8	–	ns	–
SS_SMII CLK_RX Low Period	t_{CKL}	–	4	–	ns	–
SS_SMII CLK_RX High Period	t_{CKH}	–	4	–	ns	–
Rxdata/RxSync setup to CLK_RX rising edge	t_{DS}	1.5	–	–	ns	–
Rxdata/RxSync hold from CLK_RX rising edge	t_{DH}	1	–	–	ns	–

4.2.11 Serial Management Interface (SDC/SDIO) Timing

SDC/SDIO timing is same as MDC/MDIO except Data Length is 32 bits.

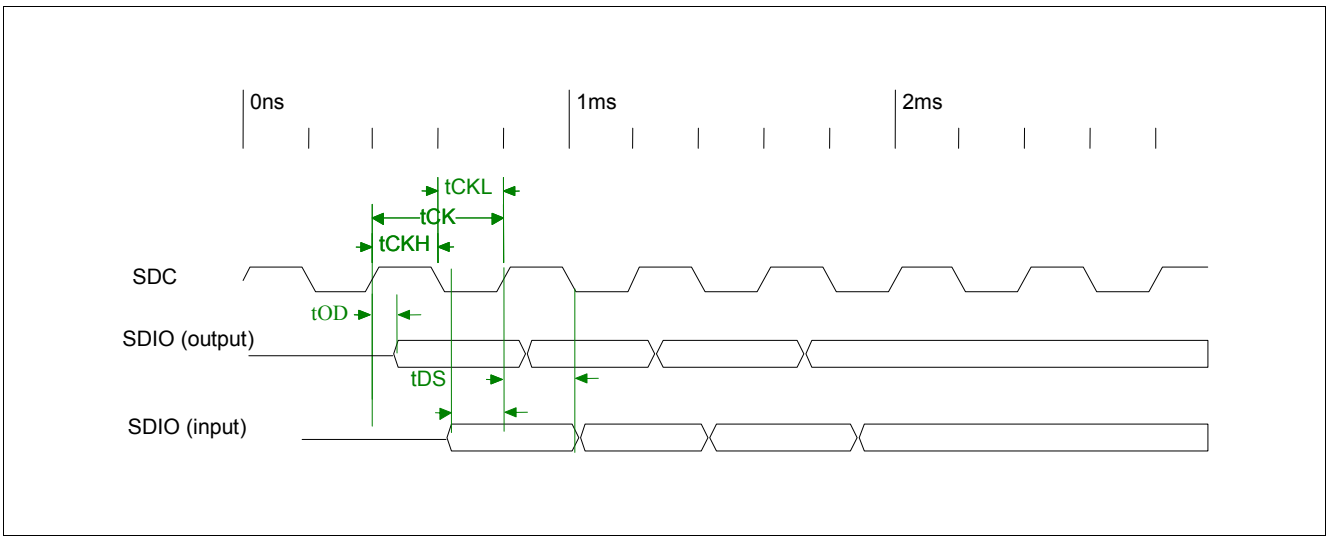


Figure 24 Serial Management Interface (SDC/SDIO) Timing

Table 54 Serial Management Interface (SDC/SDIO) Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SS_SMII CLK_RX Clock Period	t_{CK}	–	400	–	ns	–
SS_SMII CLK_RX Low Period	t_{CKL}	–	200	–	ns	–
SS_SMII CLK_RX High Period	t_{CKH}	–	200	–	ns	–
S DC to S DIO Output Delay	t_{OD}	–	–	20	ns	–
S DIO Input to S DC Setup Time	t_{DS}	10	–	–	ns	–
S DIO Input to S DC Hold Time	t_{DH}	10	–	–	ns	–

5 Package Outlines

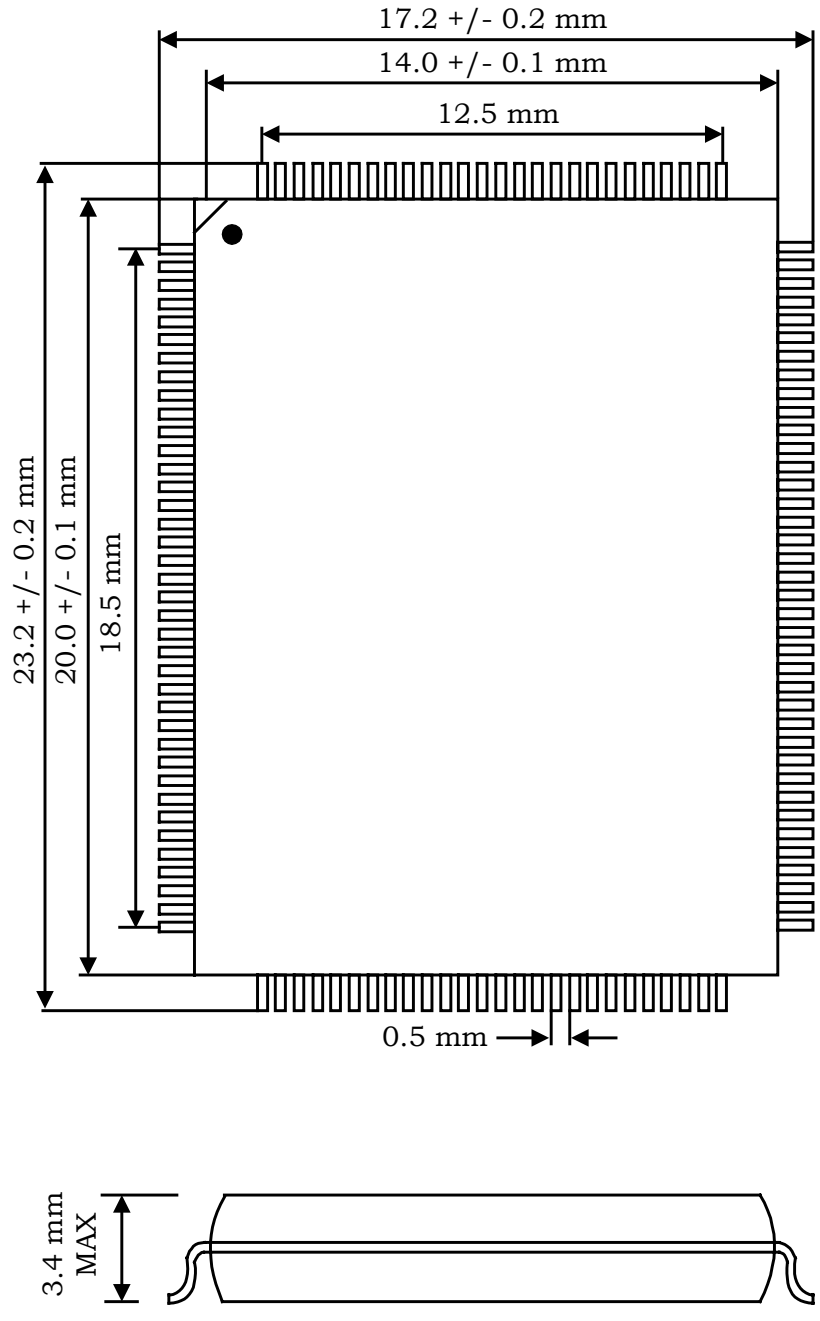


Figure 25 **P-FQFP-128-1** (Plastic Fine Pitch Quad Flat Package)

TerminologyTerminology

B	
BPDU	Bridge Protocol Data Unit
C	
CRC	Cyclic Redundancy Check
CRSDV	Carrier Sense and Data Valid
D	
DA	Destination Address
DUPCOL	Duplex and Collision
E	
EDI	EEPROM Data Input
EDO	EEPROM Data Output
EECS	EEPROM Chip Select
EESK	EEPROM Serial Clock
ESD	End of Stream Delimiter
F	
FCS	Frame Check Sequence
FET	Field Effect Transistor
G	
GARP	Generic Attribute Registration Protocol
GMRP	GARP Multicast Registration Protocol
GVRP	GARP VLAN Registration Protocol
I	
IGMP	Internet Group Management Protocol
IPG	Inter-Packet Gap
M	
MAC	Media Access Controller
MDC	Management Data Clock
MDIO	Management Data Input/Output
MII	Media Independent Interface
P	
PHY	Physical Layer
PLL	Phase Lock Loop
PPPoE	Point to Point Protocol over Ethernet
PVID	Port VLAN ID
Q	
QFP	Quad Flat Pack
QOS	Quality of Service
R	
RMII	Reduced Media Independent Interface

S

SA	Source Address
SS-SMII	Source Synchronous Serial MII

T

TA	Turn Around
TOS	Type of Service
TTL	Transistor Transistor Logic

U

UNIQUE	Universal Queue management

V

VID	VLAN ID
VIH	Voltage Input High
VIL	Voltage Input Low
VLAN	Virtual LAN

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